STRESS ANALYSIS OF SILICON CARBIDE MICROELECTROMECHANICAL SYSTEMS USING RAMAN SPECTROSCOPY

THESIS

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AFIT/GMS/ENP/03-01

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THESIS

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Stanley J. Ness, B.S.M.E.

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List of Abbreviations

Abbreviation Page

MEMS (Micro-Electro-Mechanical Systems) 1

SiC (Silicon Carbide) 1

DoD (Department of Defense) 1

Si (Silicon) 2

DRIE (Deep Reactive Ion Etching) 4

MESFET (Metal-Semiconductor-Field-Effect-Transistor) 4

MUMPs (Multi-user MEMS Processes) 5

GaAs (Gallium Arsenide) 5

MEMCAD (MEM Computer Aided Design) 5

MUSiC^{SM} (Multi-user Silicon Carbide Surface Micromachining) 5

SiO_2 (Silicon Dioxide) 6

Si_3N_4 (Silicon Nitride) 6

IFM (Interferometer Measurement) 6

APCVD (Ambient Pressure Chemical Vapor Deposition) 8

GaN (Gallium Nitride) 9

CWRU (Case Western Reserve University) 12

CMP (Chemical Mechanical Polishing) 12

KOH (Potassium Hydroxide) 13

EDP (Ethylene Diamine Pyrochatechol) 13

SEM (Scanning Electron Microscope) 13

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HF (Hydrofluoric Acid) 14

PolySiC (Polycrystalline silicon carbide) 14

PolySi (Polycrystalline silicon)..15

LIGA (Lithographie, Galvanoformung, Abformung)......................................17

RIE (Reactive Ion Etching)...20

LTO (Low Temperature Oxide)..21

BOE (Buffered Oxide Etch)..22

PVD (Physical Vapor Deposition)..24

RF (Radio Frequency)...26

SiH_4 (Silane) 27

C_3H_4 (Propane)..27

sccm (Standard Cubic Centimeters per Minute)...27

slm (Standard Liters per Minute)...27

TEC (Thermal Expansion Coefficient)...28

FEM (Finite-element Modeling)..29

CCD (Charge Coupled Device) 36

FTA (Folded Transverse Acoustic) 40

FTO (Folded Transverse Optical)...39

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Abstract

During the fabrication of Micro-Electro-Mechanical Systems (MEMS), residual stress is often induced in the thin films that are deposited to create these systems. These stresses can cause the device to fail due to buckling, curling, or fracture. Government and industry are looking for ways to characterize the stress during the deposition of thin films in order to reduce or eliminate device failure. Micro-Raman spectroscopy has been successfully used to analyze poly-silicon MEMS devices made with the Multi-User MEMS Process (MUMPS®). Micro-Raman spectroscopy was selected because it is nondestructive, fast and has the potential for *in situ* stress monitoring. This research attempts to validate the use of Raman spectroscopy to analyze the stress in MEMS made of silicon carbide (SiC) using the Multi-User Silicon Carbide surface micromachining (MUSiC℠) process. Surface interferometry of fixed-fixed beam arrays and comb drive resonance test are employed to determine stress and compare it to the Raman values. Research also includes baseline spectra of 6H, 4H, and 15R poly-types of bulk SiC. Raman spectra of 1- to 2-μm thick 3C-SiC thin films deposited on silicon, silicon nitride, and silicon oxide substrates are presented as an attempt to establish a baseline spectra for 3C-SiC, the poly-type of SiC found in MEMS made with the MUSiC℠ process.

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Chapter 1: Introduction

The material properties of silicon carbide (SiC) make it a prime candidate in the search for a better high-temperature, high-frequency, and extreme-environment semiconductor. The Air Force is very interested in developing microelectromechanical systems (MEMS) for extreme environments to enhance the performance of aircraft engines, space-based platforms, and smart munitions. The process of fabricating SiC MEMS often leaves undesirable stress concentrations in the thin films that make up these microscopic systems, resulting in failure of the device. This thesis explores the potential for Raman spectroscopy to characterize these stresses, with the objective of discovering the best way to alleviate undesirable stress concentration in SiC MEMS.

1.1 Motivation

Since the end of World War II, the development of modern electronic devices has seen resounding success. A prime example is the computer industry, where a decrease in the cost of manufacturing integrated circuits has put a personal computer at the tips of nearly everyone's fingers. However, the demand for solid-state devices that can perform their intended function in an environment other than the home or office is increasing.

The Department of Defense (DoD) is particularly interested in more robust solid-state control devices for use in aircraft, satellites, and munitions. Silicon and other

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commonly used semiconductors are limited by their operating temperature and mechanical properties from use in high temperature, high power, high voltage and high g-force environments. Modern jet aircraft rely heavily on sensors and on-board computers to enhance their efficiency and capabilities. Many of these electronics monitor and control vital engine components and control surfaces that operate at high temperatures. However, due to the shock and temperature limitations of silicon-based electronics, they must be located in environmentally controlled areas. This requires running wire from the electronics to the high temperature sensors and controls. In some instances, fuel flowing into the engine compartment has been used as a coolant for these electronic devices. But, these methods are less than perfect since they have led to a significant increase in weight, lower fuel efficiency and added complexity that has created reliability and maintenance problems. SiC electronics that have a maximum operating temperature of approximately 800° C could replace these sheltered electronics resulting in life-cycle cost savings, weight reduction, and increased performance and reliability. [1]

There are many material properties that make SiC very attractive for integrated circuit and MEMS applications. SiC, with a breakdown voltage that is eight times higher than silicon (Si), would eliminate the need to harden micro-circuitry against electro-magnetic-pulse, directed-energy weapons, and cosmic events. Its high operating temperature would allow sensors to be made that could be mounted in jet engine compartments. Figure 1.1 shows the plan view of a 4-mm-wide SiC micro pressure sensor that can operate at temperatures up to 400° C. [2]

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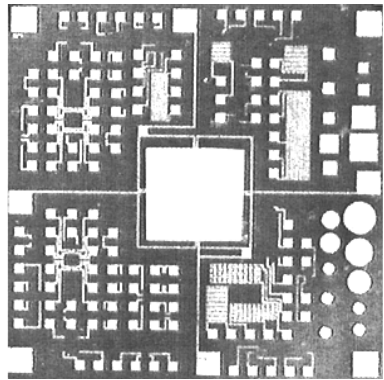

Figure 1.1: SiC piezo-resistive micro-pressure sensor [2]

Figure 1.2 shows a typical lateral resonator fabricated by PolySiC surface micromachining. The device uses suspension beams that are 2-µm-thick PolySiC by 3-µm wide and 100-µm to 200-µm long. With resonance operation has high as 900° C, the actuation voltage was as low as 30 V and resonant frequencies ranged from 30-60 kHz, depending on geometry. [2]

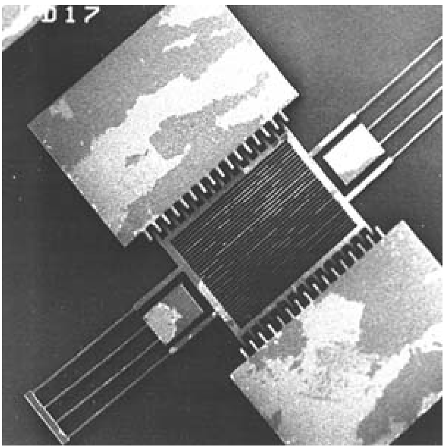

Figure 1.2: PolySiC electrostatic micro-actuator [2]

Figure 1.3 shows the swirl chamber and exit orifice of a micro-machined fuel atomizer. After fabrication of the atomizer pattern using Deep Reactive Ion Etching

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(DRIE), the Si microstructure was coated with layer of SiC. Both coated and uncoated atomizers were tested for erosion. The uncoated atomizers had their edges rounded by erosive wear near the exit orifice edge, whereas coated atomizers showed no evidence of edge rounding. Additionally, uncoated atomizers are more likely to break and chip upon handling. [2]

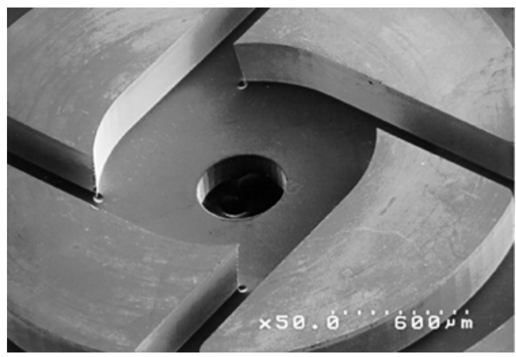

Figure 1.3: Micro-machined fuel atomizer conformally coated with SiC [2]

In the last decade alone, SiC devices such as P-N junction diodes, Schottky barrier diodes, rectifiers, and MESFETs have been developed. Each of these is capable of operating in the high voltage (4500 Volts), high temperature (600° C) or high frequency (3 GHz) range. [3]

These are just a few of the examples of where this technology is headed. With the vast number of weapon systems and satellites that rely heavily on electronics or operate under extreme conditions, it is not difficult to see the cost savings and strategic edge SiC can deliver to national defense.

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1.2 Background

This thesis constitutes a partial continuation of research begun by L.A. Starman in his Ph.D dissertation entitled, Characterization of Residual Stress in Microelectromechanical Systems (MEMS) Devices using Raman Spectroscopy. In his research, he used micro-Raman spectroscopy to measure the residual and induced stresses in MUMPs® processed PolySi and GaAs MEMS devices. Raman spectroscopy line and mapping scans were collected to obtain Raman residual stress profiles on unreleased and released MEMS fixed-fixed beams, cantilevers, and micro-mirror flexures. These profiles were compared to finite element analysis models to assess the realization of the Raman stress profiles. Finite element residual and induced stress profiles were obtained from MEMCAD and used to assess the viability of micro-Raman spectroscopy as an *in situ* stress measurement technique. Micro-Raman spectroscopy was selected since it is nondestructive, fast and provides the potential for *in situ* stress monitoring. [4]

This thesis attempts to duplicate some of the same results but for SiC MEMS in place of PolySi MEMS. FLX Micro, Inc. (formerly known as Fiberlead, Inc.) has developed a method similar to MUMPs® (a process whereby MEMS are machined in PolySi) for PolySiC. This process is known as the MUSiC℠ process and uses micromolding and surface micromachining techniques to form MEMS structures. Prior to finishing his dissertation, Dr. Starman designed and submitted plans for test devices to FLX Micro, Inc. that were nearly identical to those used for the PolySi research in his dissertation. These test devices included fixed-fixed beam arrays, cantilever arrays, comb drives, actuatable micro-mirrors, etc.

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1.3 Approach

The goal of this research is to validate a method of characterizing stress in thin films of SiC used to make MEMS devices. First, several different samples of bulk SiC poly-types (4H, 6H, and 15R) were obtained and the Raman spectra of each were determined using a micro-Raman system manufactured by Renishaw, Ltd. Unfortunately, a sample of bulk 3C-SiC, the poly-type typically used for SiC MEMS thin films, was not available. Next, Raman spectra were gathered from samples of PolySiC thin films on Si, Si_3N_4 and SiO_2 substrates. All of these had an aluminum mask in place on the surface of the film. When the full MUSiC^{SM} run was completed and arrived at AFIT, spectra were gathered for these chips as well, specifically on anchor points and along the length of cantilevers and beams. Then, after etching and releasing the MEMS structures on the MUSiC^{SM} chips, Raman spectra were collected again at the same locations.

To verify the residual stress results from the Raman test, other post-release tests were performed to provide useful information about the material properties of the structures. These tests include Zygo interferometer profiling to determine maximum beam length before buckling and a comb-drive resonant frequency tests. The interferometry measurements (IFM) of the buckling beam arrays are used to determine the residual stress once a value for Young's modulus is determined from the comb-drive tests.

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1.4 Overview

This thesis rests upon a foundation of theory and technology in several different areas, all of which, when brought together, make the research possible. In Chapter 2, a thorough treatment of silicon carbide, MEMS and the MUSiC^{SM} process, thin-film stress, and Raman spectroscopy are set forth. With this foundation in place, experimental procedures are explained in Chapter 3. Results and the analysis of the data are presented in Chapter 4. Finally, Chapter 5 includes any conclusions that can be drawn from the results, and several recommendations for future study are suggested. References for each chapter are listed at the end of each chapter.

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Chapter 2: Samples

This thesis requires an understanding of several different topical areas. These primarily include: the material properties of silicon carbide (SiC), microelectromechanical systems (MEMS) and the Multi-user Silicon Carbide surface micromachining (MUSiC^{SM}) process, thin film stress, the ambient pressure chemical vapor deposition (APCVD) process, micro-Raman spectroscopy, and other electronic and spectrographic characterization techniques. In this chapter, the first four topical areas will be treated at a level that will enable the reader to understand the samples being examined and the implications of the research. Micro-Raman spectroscopy will be treated in the following chapter as part of the experiment.

2.1 Silicon Carbide

For over a hundred years now, silicon carbide has been mass-produced for use as an industrial abrasive due to its near-diamond hardness of just over 9 on the Moh scale. Silicon carbide was first discovered by a Swedish scientist, Jöns Jacob Berzelius (1779-1848), while he was trying to synthesize diamonds. Then, in 1891, Edward Goodrich Acheson (1856-1931) mistakenly thought the crystals were a compound of carbon and aluminum, and in 1893 patented the trademark "carborundum" for the substance he had "discovered" and marketed as a synthetic grinding stone [3].

For the interest of this thesis, the most significant discovery was the electroluminescence of silicon carbide by the British electronics engineer Henry Joseph Round (1881-1966) in 1907. [3] Many other advances in crystal growth and applications

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have developed since silicon carbide's initial discovery. Only recently has it begun to receive serious attention as a solution for some wide-band-gap semiconductor applications.

Figure 2.1: Silicon carbide grinding stones or "carborundum" [3]

It is generally accepted that a "wide" band-gap semiconductor material has an energy gap over 2 eV. Other potential materials for the wide-band-gap role include GaN, diamond, ZnSe, and ZnO. Table 1 compares SiC to some other common semiconductors. Other than 3C-SiC (also known as beta-SiC), silicon carbide grows in several different arrangements, of which there are about 70 hexagonal and 170 rhombohedral lattice crystal structures. These are known as alpha-SiC. The most interesting for use in electronic devices and MEMS are 4H, 6H, and 3C. Figure 2.2 shows the two possible lattice structures.

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Table 1: Material properties of wide-bandgap and common semiconductors [5]

	3C-SiC	4H-SiC	6H-SiC	A-GaN	β-GaN	Diamond	Si	GaAs
Density (g/cm^3)	3.17	-	3.21	6.095	-	3.52	2.326	5.32
Lattice constant(s) (Å)	4.38	a=3.09 c=10.08	a=3.08 c=15.12	a=3.18 C=5.17	4.520	3.566	5.431	5.85
Melting point (℃)	1800(>)			1200(?)		3872	1415	1238
Thermal conductivity (W/cm·K)	3.9	3.7	4.9	1.3	-	6-10	1.5	0.54
Thermal expansion coefficient (10^{-6}/K)	2.9	-	4.3	a=5.59 C=3.17	3.17	1.0	2.1	6.0
Mobility (cm^2/V-s) electrons	1000	900	450	440-900	-	1800	1450	8500
Mobility (cm^2/V-s) hole	100	100	50	-	-	1400	450	400
E_g[300K] (eV)	2.2	3.26	3.02	3.44	3.25	5.50	1.11	1.428
Breakdown voltage (10^6/V·cm)	2.0	3.3	3.0	5.0	-	10	0.3	0.4
Band structure	Indirect	Indirect	Indirect	Direct	Direct	Indirect	Indirect	Direct
Crystal Structure	Zincblende	Wurtzite	Wurtzite	Wurtzite	Zincblende	Diamond	Diamond	Zincblende
Crystal System	Cubic	Hexagonal	Hexagonal	Hexagonal	cubic	Cubic	Cubic	Cubic
Space Group	Td2-F43m	P63mo	P63mo	P63mo		Or7-Fd3m	Or7-Fd3m	Td2-F43m

SiC exhibits a form of one-dimensional polymorphism called polytypism. SiC crystallizes in many different polytypes, which differ from one another only in the stacking sequence of a double layer. Each double layer consists of two planes of close-packed Si and C atoms (one Si atom lying directly over one C atom), and each successive double layer is stacked over the previous one in a close-packed arrangement. Notice in Figure 2.2 that each silicon atom bonds with the four closest carbon atoms, and each carbon atom bonds with the four closest silicon atoms.

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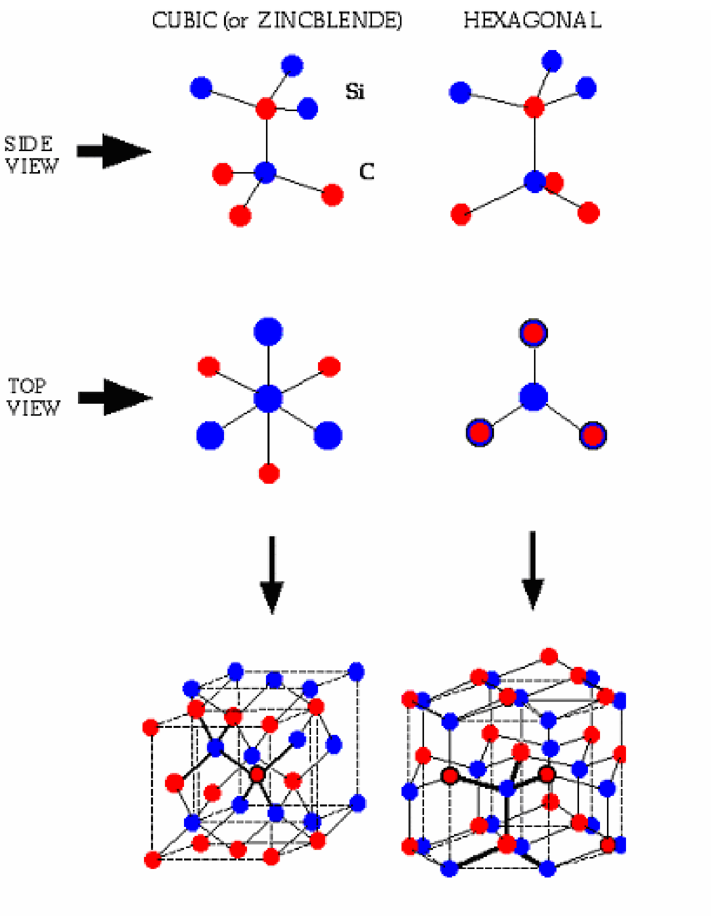

Figure 2.2: Lattice structures of SiC [6]

These polytypes are designated by the form, NX-SiC, where N is the number of stacked layers before the pattern repeats itself and X is the crystalline arrangement. Since 3C-SiC is arranged in a Zinc-blende structure, it can be grown on a silicon substrate. [2]

Silicon, GaAs, and Ge have had the spotlight in the semiconducting realm because they are easier and cheaper to grow as relatively pure, bulk crystalline ingots. Wafers cut from these ingots are nearly defect free and readily doped with impurities in order to make transistors, diodes, or other electronic devices. They are also easily etched with chemicals, so machining MEMS structures out of PolySi is also a relatively easy and

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inexpensive affair. In contrast, the material properties that make SiC such a desirable semiconductor also create problems in its manufacture and processing. Hence, a great deal of effort and creativity has gone into finding ways to manufacture electronic devices and MEMS from SiC in the cheapest way possible. Case Western Reserve University (CWRU) and FLX Micro, Inc. have pioneered one such effort.

2.2 MEMS and the MUSiC^{SM} process

The Multi-user Silicon Carbide surface micromachining (MUSiC^{SM}) process is an eight-mask MEMS fabrication process using chemical vapor deposition at ambient pressure to deposit polycrystalline silicon carbide (PolySiC) for the structural layers. The process creatively combines a few different techniques used in MEMS fabrication. These include bulk micromachining, surface micromachining, micromolding, and chemical-mechanical polishing (CMP). This section will describe these techniques.

2.2.1 SiC Use in Bulk Micromachining of Si

Because of its outstanding electrical and mechanical properties, SiC is becoming the material of choice for high-temperature solid-state transducers. With new methods that will be detailed in the next section, large-area silicon substrates can be used to grow thin films of 3C-SiC. Being able to deposit thin films on semiconducting material is the first step in MEMS fabrication. The fact that it can be done on a relatively large wafer is significant since this is required for batch fabrication and to be economically competitive. CWRU was the first to successfully deposit a spatially uniform film of 3C-SiC on a 4-

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inch (100) silicon wafer. [2] It is upon these wafers that bulk micromachining structures like diaphragms and cantilevers can be created.

Etchants like KOH and ethylene diamine pyrochatechol (EDP), that are commonly used to machine PolySi layers, cannot be used to form SiC structures in the bulk since it is highly resistant to such corrosive fluids. Instead, reactive ion etching (RIE) with a C_2F_6/O_2 plasma and an aluminum mask is used. First, SiC is deposited to the desired thickness, etched with RIE and then polished to a mirror finish. Next it is cleaned and thermally oxidized. This creates a 1.5-µm-thick layer of silicon dioxide on the backside of the silicon substrate and slight oxidation of the SiC surface. The 1.5-µm-thick layer of silicon dioxide is patterned using standard photolithography techniques to create an etch mask for diaphragms, beams and cantilevers. Any silicon dioxide on the 3C-SiC surface is removed by wet chemical etching in HF. Finally, SiC diaphragms are made by etching the unmasked regions of the silicon substrate in a KOH/H_2O solution. Figure 2.3 shows the process flow and Figure 2.4 shows an SEM image of the diaphragms and bridges created with this bulk micromachining technique. [2]

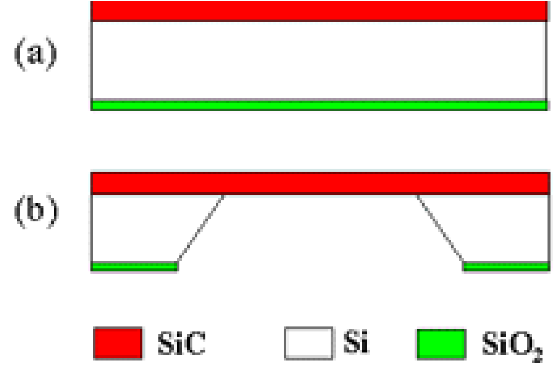

Figure 2.3: Bulk SiC micromachining process [2]

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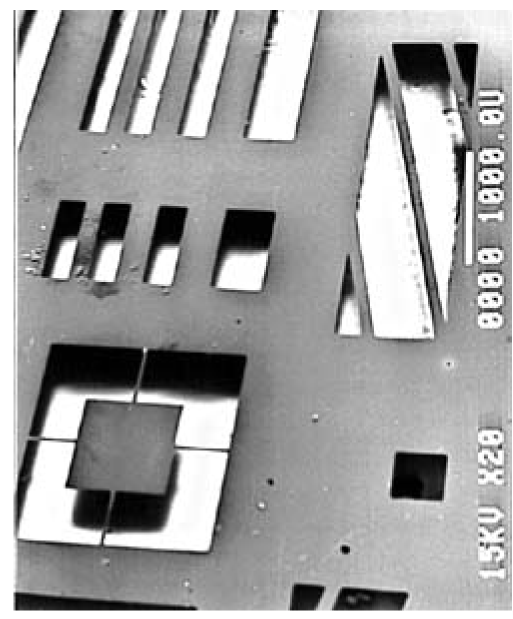

Figure 2.4: SEM image of bulk SiC micromachined structures [2]

2.2.2 PolySiC Surface Micromachining

The top surface of PolySiC can be successfully micromachined using two methods: (1) using a PolySi sacrificial layer with KOH as the release etchant, and (2) using a SiO_2 sacrificial layer with HF as the release etchant. Both use RIE to pattern the PolySiC structures just like one would for the bulk case in the previous section. Figure 2.5 shows the process flow for the first method, and Figure 2.6 shows the process flow for the second method.

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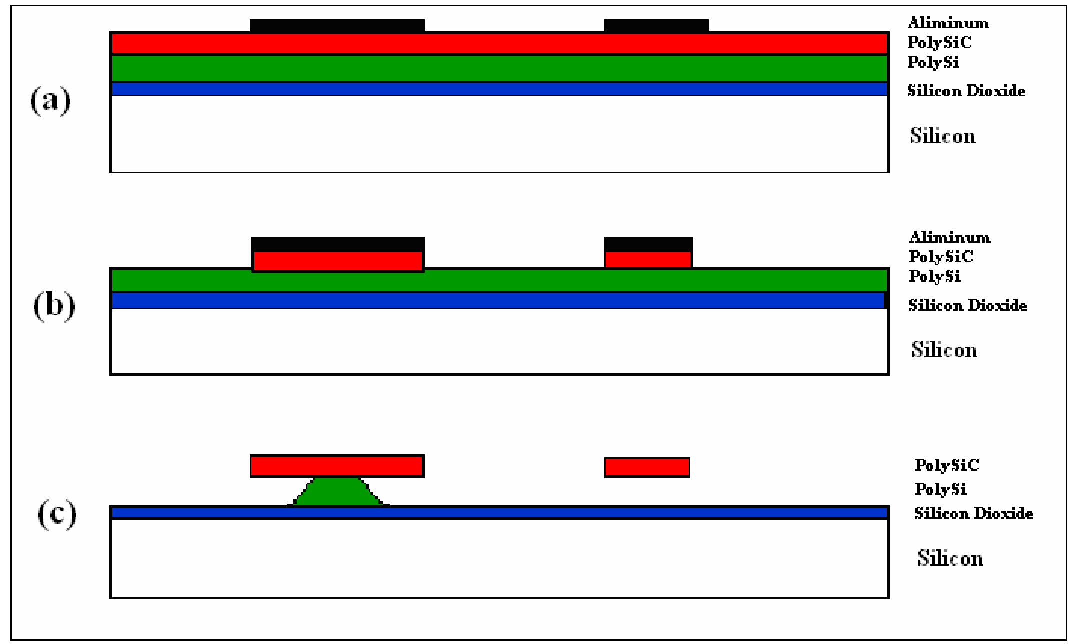

Figure 2.5: PolySiC surface micromachining with PolySi sacrificial layer [2]

The method with PolySi as the sacrificial material starts with a crystalline Si substrate as shown in white in Figure 2.5. The substrate is first coated with a layer of SiO_2 by thermal oxidation to protect the Si substrate from the KOH etch during the release process and to provide electrical isolation between the PolySi layer and the substrate. After the SiO_2 layer is completely grown, subsequent layers of PolySi and PolySiC are grown by chemical vapor deposition. Finally, a 5000-Å-thick aluminum masking layer is deposited by sputtering. Then, the aluminum mask is defined and patterned using conventional ultraviolet photolithography and wet-chemical etching, respectively. This completes step (a) in Figure 2.5. Step (b) shows PolySiC microstructures defined by RIE in a CHF_3/O_2 (97%/3%) mixture. This etch is reasonably anisotropic with an etch rate of approximately 400 Å/min. Next, the aluminum mask is removed using an HF solution. Finally, the PolySiC microstructures are released by

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selectively etching the PolySi sacrificial layer in 40 wt% KOH at 40°C; the etch rate is approximately 6 μm/hr. The etching time is controlled so that the PolySi sacrificial layer is etched from everywhere, but the anchor regions underneath the PolySiC devices. [2]

The second method is very similar to the first but uses only one layer of SiO_2 as a sacrificial layer. The Al masking and reactive ion etching of SiC is the same. The main difference is that a 48% solution of HF is used to release the free standing structures by removing the sacrificial layer.

There are three main reasons for using this kind of SiO_2 sacrificial layer process instead of the PolySi sacrificial layer process previously described. First, a CMOS-compatible (after being passivated with nitride) release etchant (HF), which does not attack Si, can be used. Second, the release layer provides electrical isolation between electrostatic device elements. Finally, this process is similar to the standard PolySi surface micromachining process. [2]

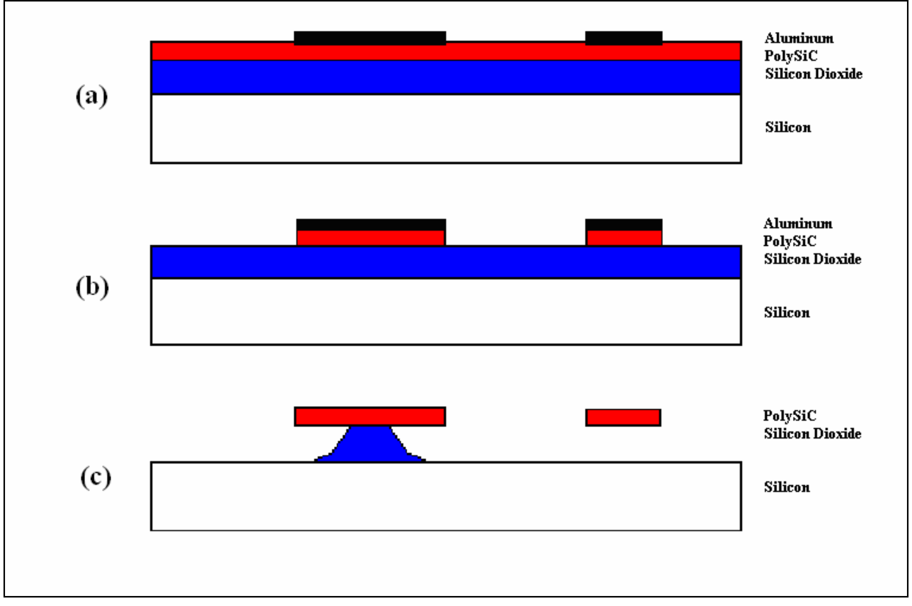

Figure 2.6: PolySiC surface micromachining with SiO_2 sacrificial layer [2]

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2.2.3 SiC Micromolding

Micromolding is a MEMS processing technique that uses a sacrificial material to create a mold. The mold is created with standard masking and UV lithography techniques. Once the mold is created, it is filled with the material from which the final device will be made. Then, the mold is dissolved with a solvent and the desired structural part remains. A similar technique was developed in Germany by Ehrfeld, *et al.* in 1986 and is know as "Lithographie, Galvanoformung, and Abformung" or LIGA. [7]. Figure 2.7 illustrates the LIGA process and is given as an example to assist the reader in understanding the micromolding process.

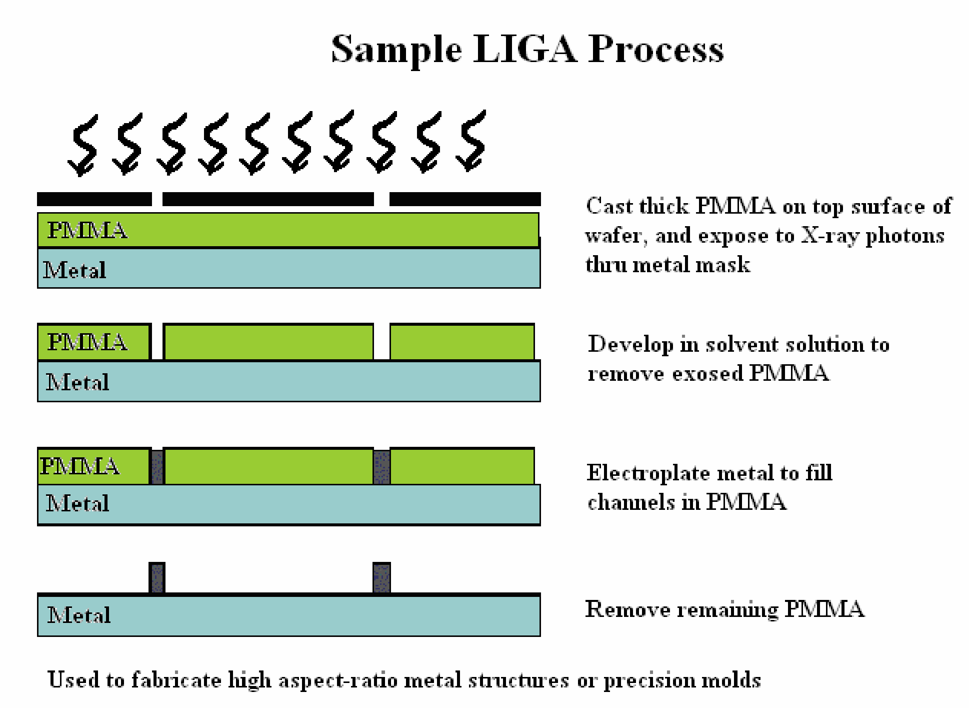

Figure 2.7: Sample LIGA process for metal [8]

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Silicon carbide can be micromolded in the same manner. First, a mold is created in PolySi or SiO_2 with photolithography and wet etching. Then, the mold is filled with 3C-SiC until the mold is completely filled. Next, the excess 3C-SiC is chemically mechanically polished until the surface of the mold is completely exposed. Finally, as in Figure 2.7, the mold is etched away leaving the SiC structure behind.

2.2.4 Chemical Mechanical Polishing

Chemical Mechanical Polishing (CMP) is a process that employs chemical etching to increase the mechanical removal rate of a semiconducting material until it is rendered smooth, planar, and the desired thickness. CMP is commonly used to polish high spots on semiconductor wafers or on films that are deposited on wafers. This is often referred to as planarization. The chemical reaction that increases the mechanical removal rate is tailored to provide a higher removal rate of one material over another.

SiC is particularly challenging to polish due to its chemical inertness. Traditionally, diamond grit compounds and water have been used to "polish" SiC wafers. But, this is purely a mechanical process and often leaves the surface too rough for good adhesion and PolySiC layer growth. However, J. Anthony Powell (High Temperature Integrated Electronics and Sensors (HTIES) team at NASA) [9] and Dr. Pirouz Pirouz (Case Western Reserve University (CWRU)) [9] developed a CMP technique for removing the subsurface polishing damage prior to epitaxial growth of the single-crystal SiC films. This technique uses a polishing procedure with an alkaline ($pH > 10$) slurry of colloidal silica at elevated temperatures (about 55° C). Surfaces of SiC wafers prepared

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with and without this type of CMP are shown in Figure 2.8 below. [9] Figure 2.9 shows the system used to polish the wafers at CWRU.

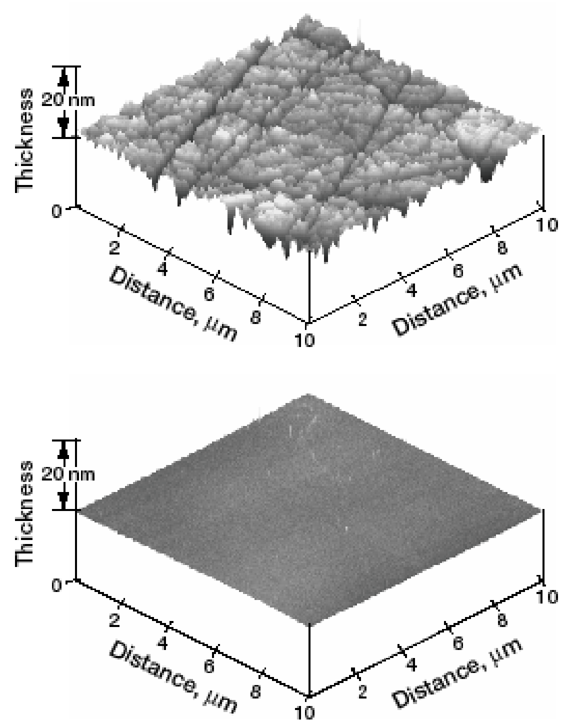

Figure 2.8: Atomic Force Microscope images of SiC wafers. Top: As-received commercial wafer. Bottom: Same wafer after CMP. [9]

Figure 2.9: Chemical mechanical polishing system at CWRU. [2]

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Films grown on SiC surfaces using this method of CMP had "significantly fewer morphological defects than films prepared on conventionally polished wafers. [This] CMP technique is still in an early state of development and much work remains before a commercially viable process can be produced." [9]

2.2.5 The MUSiC^SM Fabrication Process

FLX Micro, Inc. and Case Western Reserve University developed the MUSiC^SM process to become the easiest and most cost effective means of fabricating SiC MEMS. The key to this is a less costly prototyping directly in SiC. This is achieved because several different designs can be formed on the same wafer, thereby lowering cost through economy of scale. After processing, the wafer is diced and individual designs are sent to those who designed them. [10]

This process itself creatively combines micromolding, surface micromachining, and CMP for the MEMS structures. From the Multi-User Silicon Carbide (MUSiC^SM) Design Handbook, Version 2.0, Figures 2.10 to 2.19 show schematic cross-sections that illustrate the MUSiC^SM process in the context of building a silicon carbide (SiC) micromotor with a flange bearing design. These figures are not to scale, and the films deposited on the backside of the wafer as a result of the chemical vapor deposition process are not shown. In each step that includes photolithography, the mask name is noted in **bold**. The SiC-0, SiC-1, and SiC-2 layers are created by micromolding and chemical mechanical polishing (CMP). Only the SiC-3 is machined with the traditional dry etching technique known as reactive ion etching (RIE). [10]

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Micromolding is accomplished by depositing a sacrificial mold material (silicon dioxide or polysilicon) then etching a "reverse" pattern of the intended SiC structure into the mold material. Next, the SiC film is deposited to fill the mold. CMP is then performed to remove SiC from the "field" areas (i.e., on top of the mold), resulting in a planar surface. The resulting films contain the desired pattern in SiC surrounded by the sacrificial layer. The RIE technique used to form the SiC-3 layer is explained previously in Section 2.2.2.: SiC Surface Micromachining. [10]

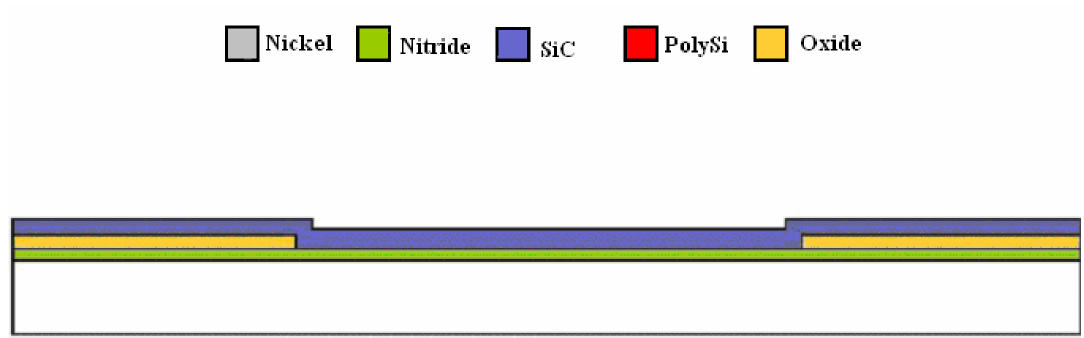

Figure 2.10: Step 1. The starting substrate is a 100 mm diameter silicon wafer, *p*-type, 1-10 Ω-cm resistivity. First, a 0.6 μm-thick layer of low-stress silicon nitride is deposited. Next, a 0.5 μm-thick low temperature oxide (LTO) is deposited and patterned to create the mold for the SiC-0 layer (mask **SiC-0**). The 0.5 μm-thick SiC "shield" layer (SiC-0) is then deposited over the oxide mold. [10]

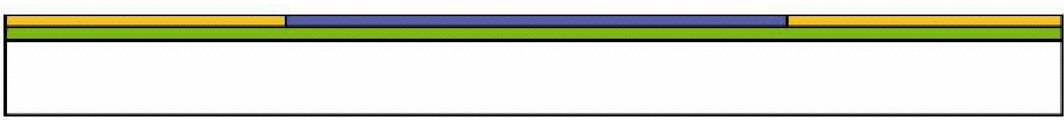

Figure 2.11: Step 2. The SiC-0 layer is polished using chemical-mechanical polishing (CMP) until the SiC-0 is coplanar with the surface of the oxide mold. [10]

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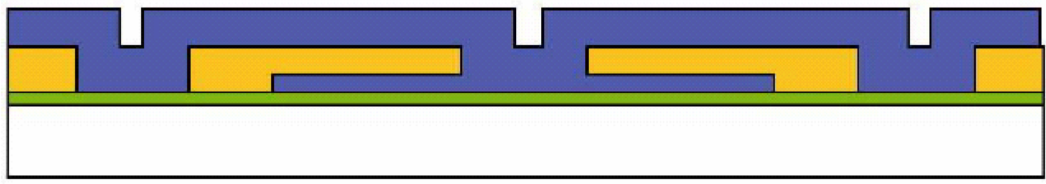

Figure 2.12: Step 3. A 2 μm LTO is deposited and patterned to create the second oxide mold for the SiC-1 layer (mask **Anchor 1**). Then, the 2 μm-thick “anchor” layer (SiC-1) is deposited. Note that SiC-1 cannot be used as a movable structural layer. [10]

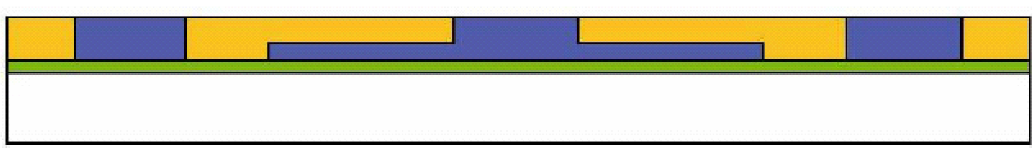

Figure 2.13: Step 4. SiC-1 is polished until it is coplanar with the second oxide surface using CMP. Note that SiC-1 is anchored to the silicon nitride if no SiC-0 feature is underneath. [10]

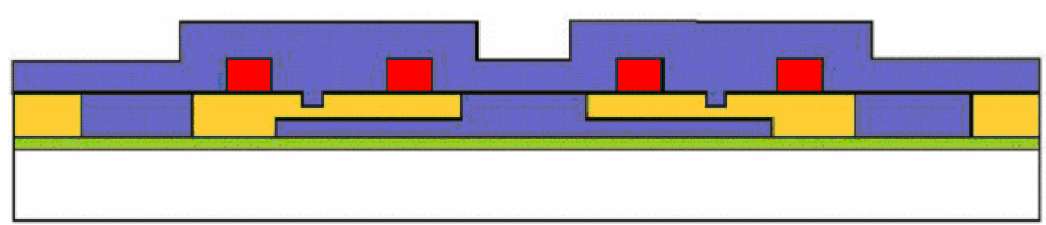

Figure 2.14: Step 5. Bushings are defined and etched (using BOE, and therefore isotropic in nature) into the second LTO mold to a depth of 7500 Å (mask **DIMPLE**). A 2 μm sacrificial polysilicon layer (Poly-1) is deposited and patterned to create the third mold (mask **SiC-2**). The 2 μm-thick SiC-2 film is then deposited over the polysilicon mold. [10]

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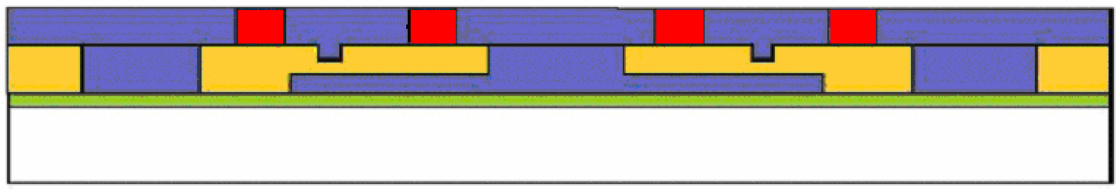

Figure 2.15: Step 6. SiC-2 is polished using CMP until it is coplanar with the polysilicon mold. [10]

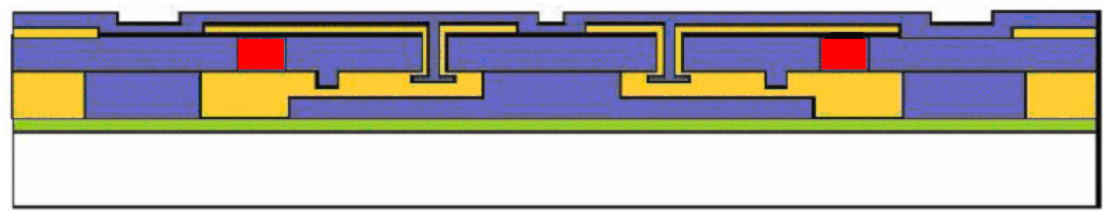

Figure 2.16: Step 7. Poly-1 is selectively removed to open access down to the first oxide (mask **Anchor 2**). A 0.75 µm-thick oxide is deposited to encapsulate the SiC-2 layer. This oxide is then patterned to open up contact areas to SiC-2 (mask **SiC2_SiC3_VIA**). Then, a 1.5 µm-thick SiC "cap" layer (SiC-3) is deposited. Note that the SiC-3 conformally coats the under etched regions created using Anchor 2. [10]

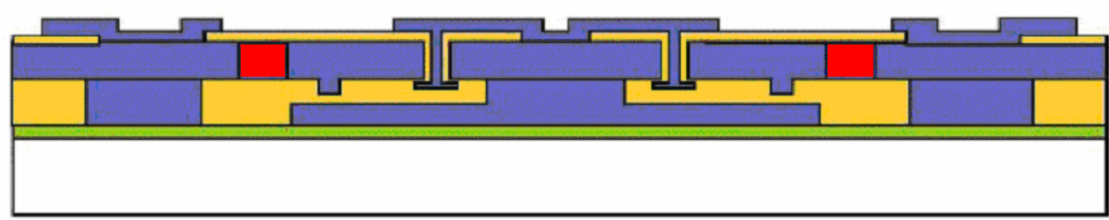

Figure 2.17: Step 8. SiC-3 is patterned and etched using RIE (mask **SiC-3**). [10]

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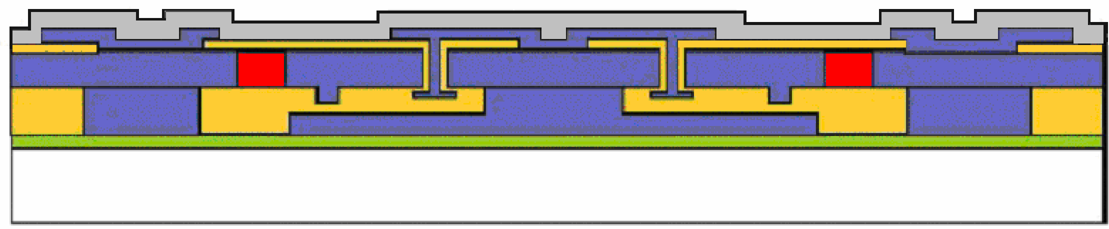

Figure 2.18: Step 9. A 0.75 μm nickel layer (metal-1) is deposited by PVD to create an ohmic contact to the SiC structures. [10]

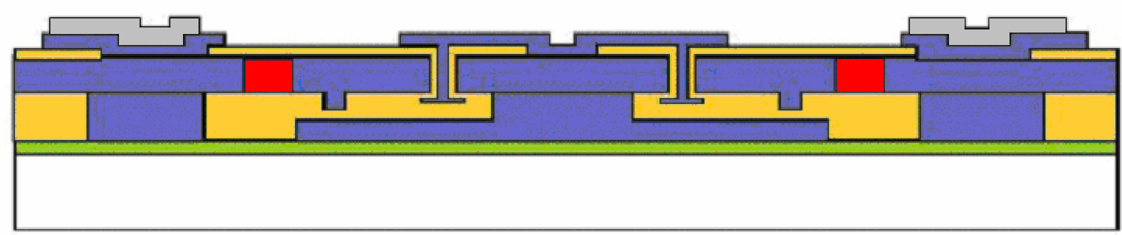

Figure 2.19: Step 10. The Metal-1 is patterned and etched, and the device is ready for dicing and release (mask **METAL-1**). [10]

"To release the structural devices, a three-step release process is required: an oxide removal (e.g., in HF), removal of the sacrificial polysilicon (e.g., using KOH), and then the final oxide is removed (e.g., in HF)." [8] Table 2 lists the different layers, their respective thicknesses and their photolithographic layer designations. Where a mold is used to pattern a layer, the mold material is also listed. From the table, "SiC-0 is used to create a ground plane, SiC-1 is used to anchor the upper SiC layers (and cannot be used to make free standing structures), and finally, both SiC-2 and SiC-3 are the structural layers used to create freestanding devices." [10]

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Table 2: Layer names, thickness and lithography levels for the MUSiC^{SM} fabrication process. [10]

Material Layer (mold, if used, is noted in parentheses)	Thickness (microns)	Lithography Level Name(s)
Silicon Nitride	0.6	-
SiC 0 (first oxide mold)	0.5	SIC0 (HOLE0)
SiC 1 (second oxide mold)	2.0	ANCHOR1, DIMPLE
SiC 2 (first poly mold)	2.0	SiC2 (HOLE2)
Third oxide	0.75	ANCHOR2, SiC2_SiC3_VIA
SiC 3	1.5	SiC3 (HOLE3)
Metal	0.75	METAL (HOLEM)

For the MUSiC-01 run, no patterning of the initial silicon nitride layer is available to allow for anchoring of structures directly to the substrate. Also note that any SiC or polysilicon depositions will deposit material on the backside of the wafer due to the vertical orientation of the wafers during chemical vapor deposition. [10]

2.3 Sources of Thin Film Stress

If the residual stress in these SiC MEMS devices is too great, it can cause cantilevers to flex up or down and bridges to buckle or resist flexing to a greater degree. Unless determined during processing, residual stress in the structures will not manifest itself until after the structures are released, when consequently, it is too late and the MEMS device would be useless for its intended purpose.

Residual stress is a by-product of the manufacturing process. Since the PolySiC lattice within the SiC structural layers is deposited on crystalline silicon, silicon nitride or

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a silicon dioxide substrate, there is a mismatch in the lattice constants, which results in voids and defects. This section will briefly explain the ambient pressure chemical vapor deposition (APCVD) process and the mechanism of induced stress during this process.

2.3.1 Ambient Pressure Chemical Vapor Deposition (APCVD)

An APCVD technique was developed at Case Western Reserve University to deposit 3C-SiC on 4-inch diameter (100) silicon substrates. Two wafers can be loaded for deposition in a cold-wall, vertical-geometry, radio frequency (RF) induction-heated reactor (Figure 2.20). The reaction chamber is a double-walled quartz tube with an inner diameter of about 170 mm. A susceptor, which holds the silicon wafers, is mounted on a quartz tube, which is mounted to the base-plate of the chamber. This piece is attached to a platform, which can be raised or lowered to insert or remove the susceptor from the chamber. A 50-kW RF generator with a ten-turn induction coil is used to heat the chamber. All gases flow into the reactor via a single line at the top of the chamber. The two gases used in the process are propane (15% propane in hydrogen) and silane (5% SiH_4 in hydrogen). Argon is used as the purge gas since nitrogen is a donor impurity in SiC. The system can deposit PolySiC layers that are undoped, or doped with phosphorus or boron. All gases are vented through the base-plate. [2]

Prior to the deposition process, the chamber is evacuated to below 100 mTorr, then backfilled to atmospheric pressure with ultra-high purity argon to flush the reactor of any gaseous contaminants. There are three steps in the process, they are: 1) an *in situ* hydrogen etch, 2) the formation of a carbonized layer, and 3) PolySiC film growth. Following the final purge with argon, the reactor is filled with hydrogen and heated to

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1000 °C to remove the polysilicon native oxide and any other contaminant on the surface of the silicon wafers. [2]

Next, a carbonized layer is formed in preparation to grow SiC layers. This is done by heating the reactor to 1360 °C with a constant flow of propane at 84 sccm (standard cubic centimeters per minute) and hydrogen at 25 slm (standard liters per minute). As the hot gases pass over the surface of the wafer, the propane (C_3H_4) breaks down into hydrocarbon fragments that react with the silicon atoms on the surface, thus forming SiC. Once a thin SiC film is formed, the silicon can no longer react with the hydrocarbons and the process must be altered to continue SiC growth. [2]

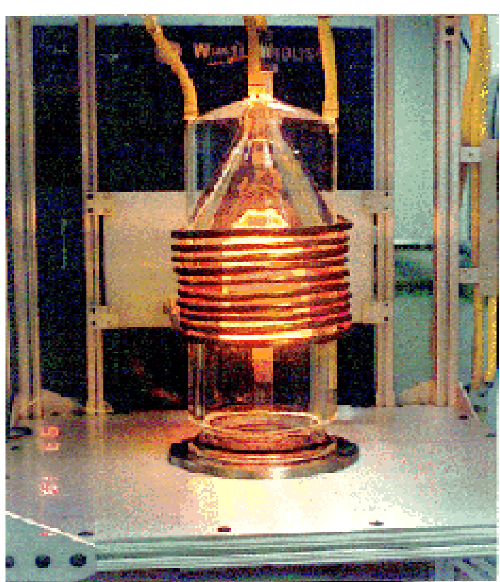

Figure 2.20: Ambient pressure chemical vapor deposition reaction chamber [2]

In the third step, the flow of propane is reduced to 26 sccm while simultaneously the flow of silane (SiH_4) is increased until a rate of 102 sccm is obtained. These temperature and flow rates are held constant for the entire growth process. Ceasing the

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flow of propane and silane terminates film growth. A flow of hydrogen is continued while the wafer cools. Finally, the chamber is purged with argon. [2]

As a side note, Figure 2.21 shows a schematic of a system at the Japan Atomic Energy Research Institute (JAERI) which is similar to the one used at CWRU. By varying flow rates of silane, propane and hydrogen, researchers at JAERI have been able to grow a single crystal wafer of 3C-SiC (non-polycrystalline). This wafer is defect free and capable of being used in robust memory devices capable of withstanding radioactive environments. [11]

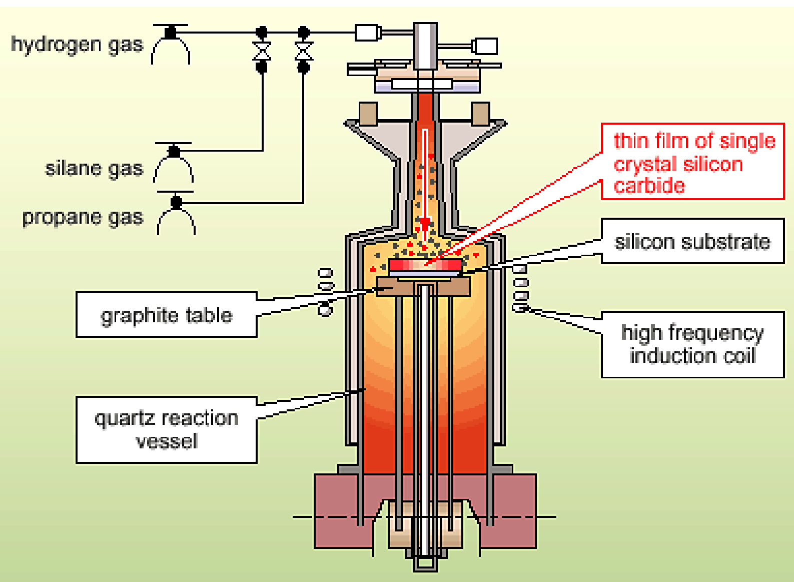

Figure 2.21: Chemical vapor deposition apparatus for growth of silicon carbide single crystal [11]

2.3.2 Induced Stress

The residual stress found in thin films of 3C-SiC deposited on silicon or a similar wafer comes from two main sources; differing lattice constants and different thermal expansion coefficients (TEC). Other sources include impurities introduced during the

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deposition process, variations in the process, and interstitial atoms or vacancies in the crystal lattice. Figure 2.22 illustrates the differences in the thermal expansion coefficients (TEC) of Si and 3C-SiC. Since the SiC deposition process occurs at a temperature of 1360 °C, the chart clearly indicates that residual stress from TEC will be measured in the PolySiC layers.

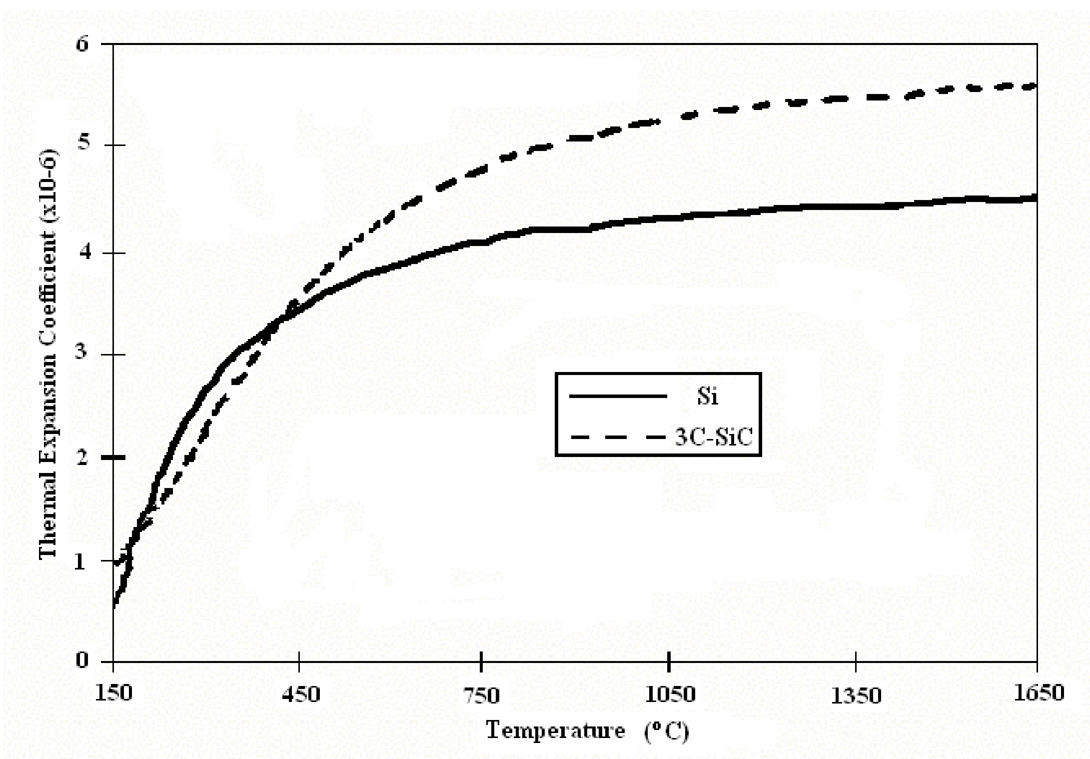

Figure 2.22: Thermal expansion coefficients for Si and 3C-SiC as a function of temperature [12]

Finite element modeling (FEM) and empirical data from research done by CWRU and the US Army Research Laboratory and NASA Glenn Research Center, Cleveland, OH quantify the amount of stress one would expect to see in 3C-SiC on Si from lattice mismatch and different TEC's. The FEM analysis predicted 259 MPa (x10^6 N/m^2)(247

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MPa after etching the substrate) due to different TEC's. Experimental measurements indicated an overall residual stress of 280 MPa. When one takes into account that there is an additional 30 – 40 MPa due to lattice mismatch, theses numbers agree quiet well. [12]

Vacancies and interstitial atoms at the grain boundaries can provide a stress relieving mechanism as the crystalline layers grow. From Figure 2.13, one can visualize that the stress through the thickness decreases as thickness increases due to defects in the lattice. As growth continues, eventually the effects of lattice mismatch are significantly overcome as to minimize the stress through the thickness. This is known as the critical thickness, t_c, and is important in calculating how thick to make MEMS structures.

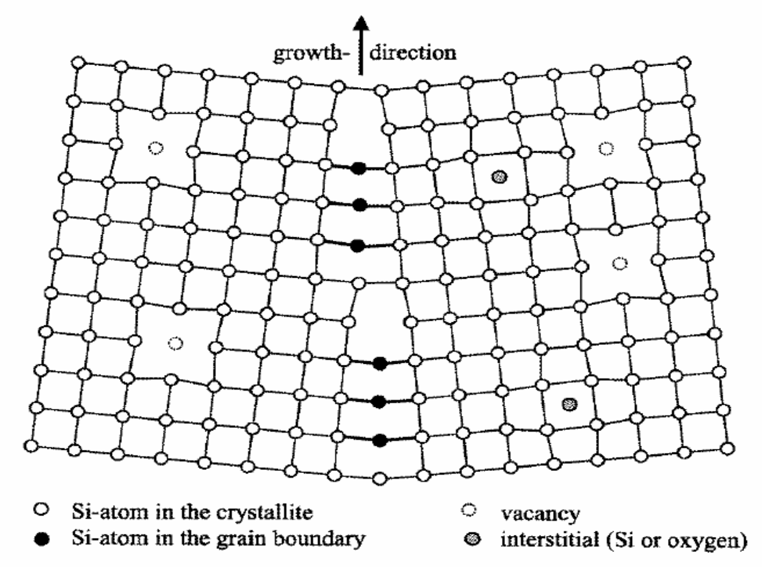

Figure 2.23: Examples of lattice defects in silicon [4]

A theoretical estimate of the critical thickness can be calculated with the following equation [13]:

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$$t_c = \frac{b(1-\nu\cos^2\beta)}{8\pi|f_o|(1+\nu)\sin\beta\cos\gamma}\ln\left[\frac{\varsigma}{b}\right] \quad (2.1)$$

where b is the Berger's vector, ν is Poisson's ratio, β is the angle between Berger's vector and the dislocation line, γ is the angle between the glide plane of the dislocation and substrate/epilayer interface, ς is a numerical factor which accounts for the energy of the dislocation ($\varsigma \approx 4$), and f_o is the misfit given by [13]:

$$f_o = 2\frac{a_{substrate} - a_{epilayer}}{a_{substrate} + a_{epilayer}} \quad (2.2)$$

where asubstrate and aepilayer are the lattice constants of the substrate and deposited layer (or epilayer), respectively. [13]

Of the two main sources, TEC-induced stress is the dominant factor, and efforts are being made to carbonize silicon at lower temperatures to reduce the amount of residual stress. As a point of interest, one research group in Italy, at the Sezione Istituto Fotonica e Nanotecnologie, is looking to grow SiC on Si wafers via a kinetic energy mechanism. [14]

2.4 Sample Description

Fortunately, a wide variety of samples were made available for study during this research, and with the preceding background, a brief description of these samples should be adequate for the reader's understanding.

The first samples to be studied were pieces of bulk crystalline wafers made of 4H-SiC, 6H-SiC, and 15R-SiC. Unfortunately, 3C-SiC was not available in bulk crystalline form. Crystalline bulk 3C-SiC is very difficult to grow and, as mentioned earlier, only

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the group in Japan has reported success in doing so. Figure 2.14 shows an example of what the 6H-SiC sample looks like. The 15R-SiC sample looked the same, only more yellow-green in color. These bulk samples were characterized with a micro-Raman system to establish a baseline of SiC polytype spectra. This information is useful for polytype recognition and Raman-shift verification. The Raman spectrum of a sample will vary somewhat between different systems, so it is important to establish a baseline for a specific system. The system available for use was made by Renishaw, Ltd., and is described in Chapter 3.

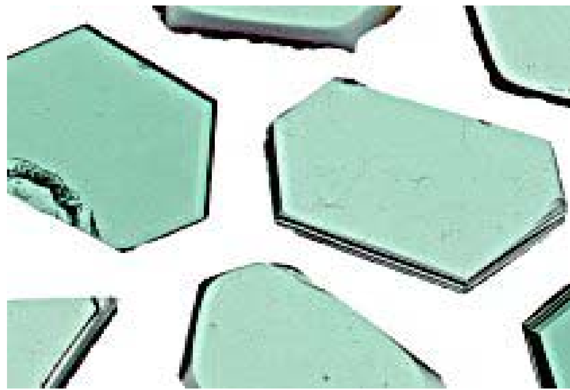

Figure 2.24: 6H-SiC crystal samples [3]

The next samples to be studied were wafers of Si, SiO_2, and Si with 1 to 2 μm of PolySiC deposited on them at CWRU via the APCVD process. The goal here was to establish a baseline Raman spectra for the PolySiC used in APCVD, a process in which the dominate polytype should be 3C-SiC. All of these samples had an aluminum mask deposited on them in preparation for etching.

The third and final type of samples tested were MEMS test chips from the inaugural MUSiC^SM run completed in December 2002. Raman spectra (of anchors,

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cantilever and beams), interferometer (Zygo), and resonance tests (on comb drives) were performed on the material and structures of these samples. The results from all the tests will be presented at length in Chapters 3 and 4. Figures 2.15 and 2.16 show a picture and an overall schematic of the chip layout, respectively.

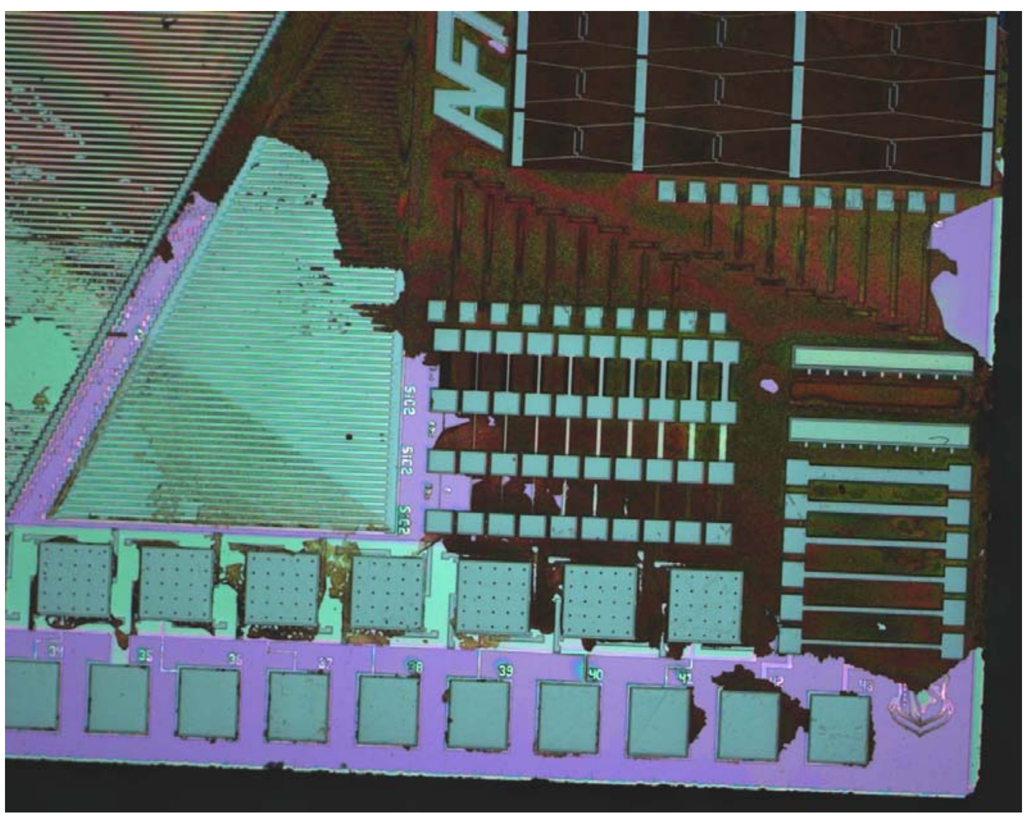

Figure 2.25: Picture of MEMS structure on AFIT test die

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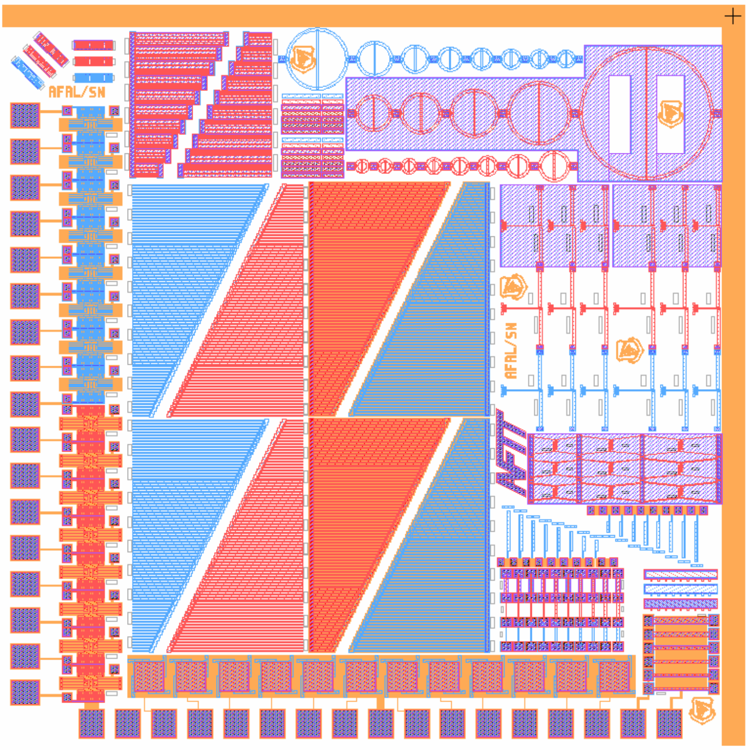

Figure 2.26: Plan view of AFIT MUSiC test die layout [15]

2.5 Conclusion

This chapter provides a comprehensive view of the samples that were characterized in this thesis. The material properties of SiC and several different techniques to fabricate MEMS out of SiC have been set forth. Since this thesis is primarily concerned with residual stress in thin-film PolySiC, the process, APCVD, whereby these thin films are grown and the sources of stress due to this process have been thoroughly described.

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Chapter 3: Experiments

This thesis conducted four different experiments on several different samples described in the previous chapter. This section will discuss in detail those experiments to include background theory, setup and procedures.

3.1 Raman Spectroscopy Theory

3.1.1 Introduction

In 1928, Venkata Raman discovered that light from a monochromatic source incident upon a specific material scattered, not only at the frequency of the incident light, but also at different frequencies. It was later determined that this was due to a momentary polarization of the electrons involved in the bonds between molecules. As the dipole relaxes, the molecule emits a bundle of vibrational energy called a phonon. This disturbance in the crystal lattice scatters the incident light based on the energy of the phonon. This is also known as Stokes scattering. Their separation from the incident frequency (Raleigh Scattering) is a direct measure of the vibrational frequencies of the sample. Therefore, different materials will produce different scattering spectra since the vibrational energy of their bonds differ one from another. From this was born the spectrographic technique known as Raman spectroscopy. Figure 3.1 illustrates a diatomic molecule under vibration scattering an incident laser beam, and the subsequent scattering.

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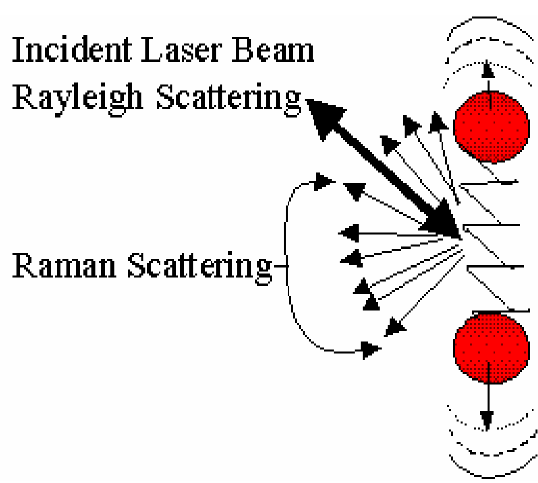

Figure 3.1: Incident beam is scattered at same frequency (Rayleigh Scattering) and shifted frequencies (Raman Scattering) [4]

Raman spectroscopy is a non-destructive, non-contact material characterization method. With the advent of charge coupled device (CCD) cameras, Fourier-transform methods, high quality diffraction gratings, and computer analysis, this technique has become a simple-to-use method for materials characterization. For example, it can be used to measure the stresses in the crystal lattices of certain materials. To do so, a laser is focused on a sample and the incident radiation is scattered by the vibrations of the crystal lattice (phonons). Residual stress in the crystal lattice will cause the phonons to vary proportionally to the strain in the lattice. [18] Thus, a slight shift in the frequency of the scattered spectrum is also observed. This makes Raman spectroscopy an effective way to monitor localized stress in MEMS devices.

Raman spectroscopy can also be used to identify the presence of different atomic bonds and crystalline arrangements. For example, the spectrum for silicon, 6H-SiC, 15R-SiC, and 4H-SiC all look different from one another. (Graphs of this can be found in Section 4.1, Raman Spectra for Bulk SiC Samples.) In this way, a sample can be

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“mapped” according to what type of material exists at a specific location within the sample. This mapping can be further localized with the use of a microscope and other optics to focus the laser beam excitation source. This is called micro-Raman spectroscopy, where in the beam is focused to a spot size of around 1-3 μm on the sample’s surface.

3.1.2 Raman System Configuration

As effective as it can be, Raman spectroscopy is not without issues that must be considered. This section will describe the specific system used in this research and some of the issues encountered. Figure 3.2 shows the basic setup of a Renishaw micro-Raman system. The laser beam (argon-ion laser at a peak wavelength of 514.5 nm for this experiment) enters from the back in the lower right-hand corner of the optics case and is immediately expanded and reflected up to point D where it is directed to the microscope objective to be focused on the sample at point A. The scattered light from the sample is then backscattered and collected 180° along the incident beam’s path to point D where the laser is filtered to reduce its intensity on the detector at point F.

The scattered light is allowed to pass through the filter and makes its way to point C where a diffraction grating separates the light for detection at point F. The CCD is linked to a desktop computer, and software algorithms are then used to interpret and plot the spectra. These algorithms use the Bragg equation (3.1) to determine the wavelength of the scattered light.

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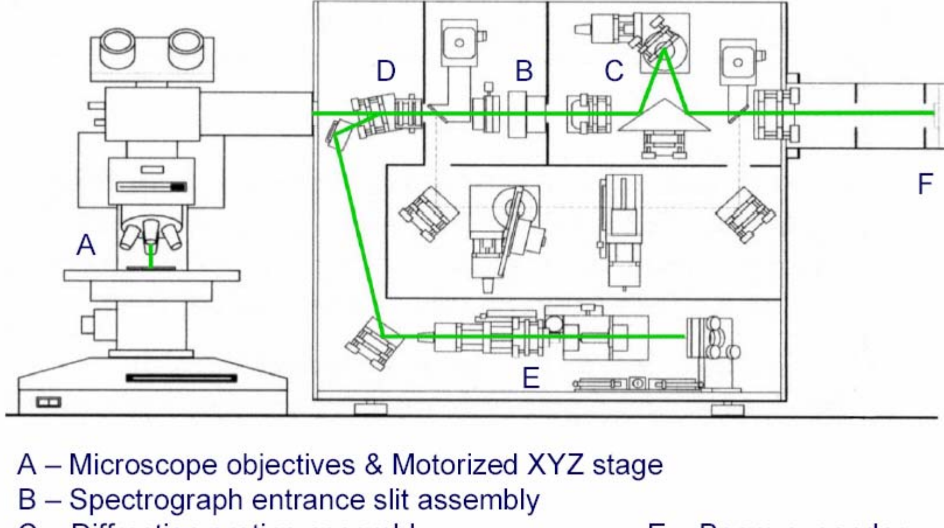

Figure 3.2: Renishaw 1000 Raman system [16]

$$d \sin \theta = m\lambda \tag{3.1}$$

In the Renishaw system, the diffraction grating (1800 lines/mm for this experiment) is mounted to a servo motor at point C. As the scattered light is collected from the sample, the motor slowly rotates the grating and reports the angle of rotation to the computer. Figure 3.3 shows how a diffraction grating can be employed in this manner.

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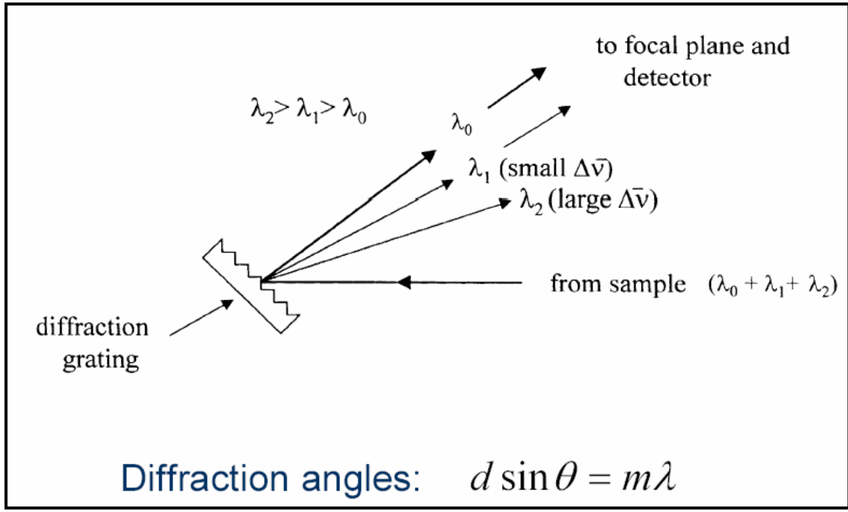

Figure 3.3: How a diffraction grating separates light into different frequencies [16]

The CCD simultaneously reports the intensity it sees for each degree of rotation. These two pieces of data are matched up and used to solve the Bragg equation (3.1) for wavelength (λ). This is then converted into wave numbers ($\bar{\nu}$) with the following relation for energy, where h is Planck's constant and c is the speed of light:

$$\bar{\nu} = \frac{1}{\lambda} \; (cm^{-1}) \qquad (3.2)$$

Now, the data is ready to be plotted in graphical form. The software can also perform numerical analysis such as curve smoothing, adding or subtracting two different spectra and other mathematical operations. Figure 3.4 is a good example of Raman data in graphical form for 4H- and 3C-SiC. Notice the sharp peaks at specific wave numbers could be used to distinguish the presence of two different polytypes in a given sample. Because of differences in the crystal arrangement, different polytypes will disperse phonons at different energies. For example, Figure 3.4 shows that 3C-SiC has sharp peaks at 796 cm^{-1} for the folded transverse optical (FTO) mode and 972 cm^{-1} for the

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folded longitudinal optical (FLO) mode. Other modes that one might see in Raman spectroscopy are the folded transverse acoustic (FTA) and the folded longitudinal acoustic (FLA). These modes can be theoretically determined with the dispersion relation specific for a given crystalline structure.

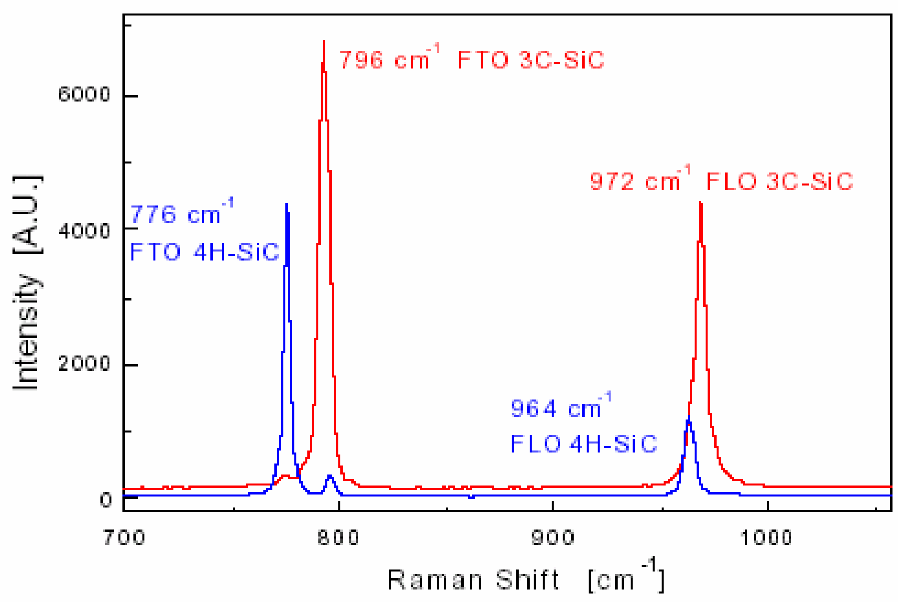

Figure 3.4: Raman spectra for 3C-SiC and 4H-SiC [17]

3.1.3 Signal Detection Issues

Getting pristine results out of a Raman system is not always easy, if at all possible. Several problems can give weak or ambiguous Raman lines or strong background noise in the collected signal. Some of these include cosmic ray events, detector saturation, fluorescence, line-broadening, and penetration depth.

Cosmic ray events are completely random in occurrence and rather benign in effect. They appear as a very sharp peak in the spectrum and are caused by high-energy particles passing through the detector at the time of data collection. They are usually

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easy to distinguish as just being out of place. The remedy is simply to perform another data collection. If the anomalous peak disappears, then it was a cosmic ray event. If not, then other sources of spectral contamination must be considered. These might include room light being reflected off the sample, laser back-scattering or a hot pixel in the CCD. [4]

Detector saturation often occurs when exposure time of the CCD is lengthened in order to bring out the Raman signal from the background noise. This problem can be seen in the output as a large peak in the spectrum that abruptly drops to zero and then just as abruptly resumes to a high peak a few wave numbers later. The remedy is to reduce exposure time or decrease laser power.

Fluorescence often manifests itself as high background noise, but is usually due to the material properties of the sample. It is often much stronger than the weak Raman scattering and can be obstructive in obtaining clear Raman data. Figure 3.5 demonstrates the difference between fluorescence and Raman scattering. A confocal microscope can eliminate mild problems with fluorescence, but if the fluorescence is too high, then the only real solution is to switch excitation sources to a laser with a longer wavelength (lower energy) that does not excite radiative transitions in the sample.

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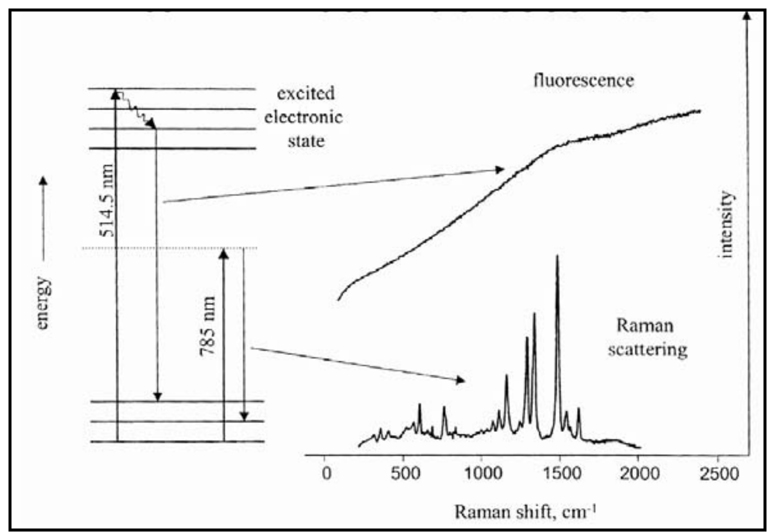

Figure 3.5: A lower energy in excitation wavelength will eliminate fluorescence [16]

In comparison to spectra from solid crystals, line-broadening often occurs in samples with a higher degree of structural disorder or high concentrations of defects. An example of this is shown in Figure 3.6 for crystalline and glassy potassium digermanate.

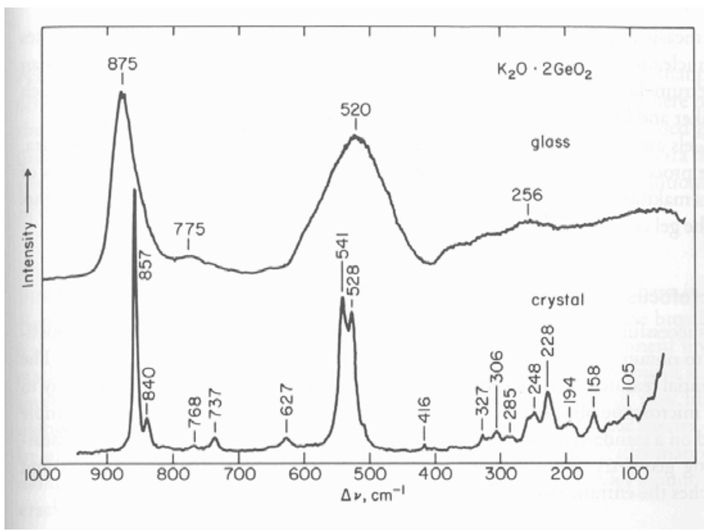

Figure 3.6: Raman spectra of crystalline and glassy potassium digermanate [18]

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The last issue to be discussed, penetration depth, is very applicable to this research. All materials are more or less transparent depending on radiation wavelength. Since MEMS devices are made of 1-2-micron thick films, we may be limited to certain wavelengths as an excitation source. If the laser excitation source has a penetration depth greater than the thickness of structure being inspected, the incident beam and the subsequent Raman scattering will extend beyond the thin film and scatter off the substrate. This will contaminate the spectra with information about the substrate underneath the structure. This may or may not be a bad thing, depending on what part of the structure is to be analyzed. Table 3 below shows absorption coefficients (α) and penetration depths (α^{-1}) for several common excitation wavelengths in the UV range for 3C-SiC. Unfortunately, a precise value for penetration depth in 3C-SiC at a wavelength of 514.5 nm is not available.

Table 3: Absorption coefficients and depth penetration for 3C-SiC [19]

Wavelength (Å)	*Laser*	*3C-SiC*			
		300 K		2 K (estimate)	
		α (cm^{-1})	α^{-1} (μm)	α (cm^{-1})	α^{-1} (μm)
3250	He-Cd	3660	2.7	3480	2.9
3336	Ar^+ ion	3190	3.1	3030	3.3
3371	N_2 gas	2970	3.4	2860	3.5
3511	Ar^+ ion	2260	4.4	2160	4.6
3540	He-Cd	2160	4.6	2070	4.8
3550	3xQ/Nd:YAG	2120	4.7	2030	4.9
3564	Kr^+	2070	4.8	1980	5.1

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3.2 Baseline and MUSiC^{SM} Raman Experiments

Raman spectra can vary slightly from system to system depending on the calibration, quality of optics, and other system-dependent parameters. To validate the system and provide a baseline of what is expected from the Raman spectra of MUSiC-01 MEMS structures, spectra from four different SiC polytypes were collected. For all scans, the diffraction grating in the Raman system described in the previous section was first calibrated at the dominate FLO silicon peak (520 cm^{-1}) using a piece of polished silicon provided by Renishaw. The calibration "zeros" the diffraction grating to the proper Raman shift according to the Bragg diffraction equation. Scan times (10 to 70 seconds) and parameters varied from run to run in order to optimize results and are included with the data in Chapter 4.

Three of the four SiC polytypes, 4H-, 6H- and 15R-SiC, were bulk crystalline samples. The fourth was PolySiC, of which the dominate polytype is assumed to be 3C-SiC. The 6H-SiC and 15R-SiC samples where highly crystalline, polished samples similar to what is shown in Figure 2.10. Both of these were placed on a polished silicon wafer while the data was taken to simulate SiC deposited on a silicon wafer as is done in the MUSiC^{SM} process. These samples were approximately 1-mm thick. The 4H-SiC was not transparent looking, but looked more like polished silicon. Only one side of this sample was polished, which was also the side on which the scans were taken. A wafer from FLX Micro, Inc. that had a 1 to 2-µm think layer of APCVD PolySiC on a silicon wafer substrate was used as a sample of 3C-SiC, since a bulk crystalline sample was not available.

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After establishing a baseline, scans of the thickest portions of the MUSiC^{SM} chips (i.e., anchor points) and of beams and cantilevers were performed. The Raman scans on a particular MUSiC^{SM} chip were performed at the same locations before and after release.

3.3 *Release Experiment*

In the MUSiC^{SM} process, the final step is to "release" the SiC structures that form the MEMS devices by chemically etching away all the sacrificial material that forms the mold for the PolySiC. This can be done with a variety of wet chemical acids or bases for the two different sacrificial materials, SiO_2 and PolySi, used in the MUSiC^{SM} process. Since the MUSiC^{SM} process is quite new and because of possible variations in layer thickness, the time tables for etching away each sacrificial layer have not been clearly defined, but guidelines from the more developed MUMPs process should be able to used. The goal of this experiment is to establish a suitable procedure for the AFIT MUSiC^{SM} test structures and provide other users of the MUSiC^{SM} process with data for perfecting the release process. For the SiO_2 layer, a solution of 48% hydrofluoric acid (HF) at room temperature was used. The equation for the reaction is as follows:

$SiO_2 + 4\ HF \rightarrow SiF_4$ (non stable) $+ 2\ H_2O$; to eliminate the non-stable process:

$SiF_4 + 2\ HF \rightarrow H_2[SiF_6]$, and thus, the overall reaction is:

$SiO_2 + 6\ HF \rightarrow H_2SiF_6 + 2\ H_2O$. [7,20]

For the PolySi layer, two fundamentally different etching processes were tried: isotropic and anisotropic wet etching. The isotropic etch is a mixture of three acids in the following ratios: 5 parts nitric acid (HNO_3):3 parts hydrofluoric acid (HF):3 parts acetic acid (CH_3COOH). This mixture also works to remove the SiO_2 layers, as well, since the

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primary mechanism here is for the nitric acid to oxidize the silicon before dissolving it in solution. The overall reaction is a complex one involving several steps. First, silicon is oxidized with nitric acid (HNO_3) and nitrous acid (HNO_2) according to the following reactions:

$$Si + 4\ HNO_3 \rightarrow SiO_2 + 4\ NO_2 + 2\ H_2O \quad \text{(slower process)}$$

$$Si + 4\ HNO_2 \rightarrow SiO_2 + 2\ H_2O + 4\ NO \quad \text{(faster process)}$$

Then, the SiO_2 is dissolved in solution by HF as described above. "The acetic acid (CH_3COOH) which is much less polar than water (smaller dielectric constant in the liquid state), helps prevent the dissociation of HNO_3 into NO_3^- or NO_2^-, thereby allowing the formation of the species directly responsible for the oxidation of silicon, HNO_2." [7,20] The overall reaction can be written:

$$18\ HF + 4\ HNO_3 + 3\ Si \rightarrow 2\ H_2SiF_6 + 4\ NO_{(g)} + 8\ H_2O \quad [7,20]$$

However, this is a simple view of a complex reaction. For a more complete explanation see [7,20].

For the anisotropic etch of polysilicon, an alkali hydroxide etchant, potassium hydroxide (KOH), was used. From the literature, where the true form of the reaction is still under debate, the overall reaction is:

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2 \qquad [7,20]$$

This too is a simple form of a complex reaction and, to better understand the chemistry, see [7,20]. What is more important to note is that this reaction will selectively etch the silicon substrate on the (100) and (110) planes as it etches the PolySi sacrificial layer in an isotropic manner. This minimizes the undesirable etching of the substrate. Also

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noteworthy is that this reaction requires water to proceed, so a higher concentration of KOH does not necessarily lead to better results.

3.4 Zygo Interferometry

Interferometers can provide very useful information about MEMS. This inspection method can provide a sharp image of the topography of the chip surface. Dr. Kevin Leedy, Air Force Research Laboratories/Sensors Directorate, performed the interferometry for this experiment. Figure 3.7 shows a picture of the system and a working schematic. From the equipment manufacturer's webpage, the following provides a brief description of the interferometer and how it works.

> The NewView 5000 is based on scanning white-light interferometry, a traditional technique in which a pattern of bright and dark lines (fringes) result from an optical path difference between a reference and a sample beam. The mechanism is simple. Incoming light is split inside an interferometer, one beam going to an internal reference surface and the other to your sample. After reflection, the beams recombine inside the interferometer, undergoing constructive and destructive interference and producing the light and dark fringe pattern. In the NewView 5000, a precision vertical scanning transducer and camera together generate a three-dimensional interferogram of the surface, processed by the computer and transformed by frequency domain analysis resulting in a quantitative 3-D image. [21]

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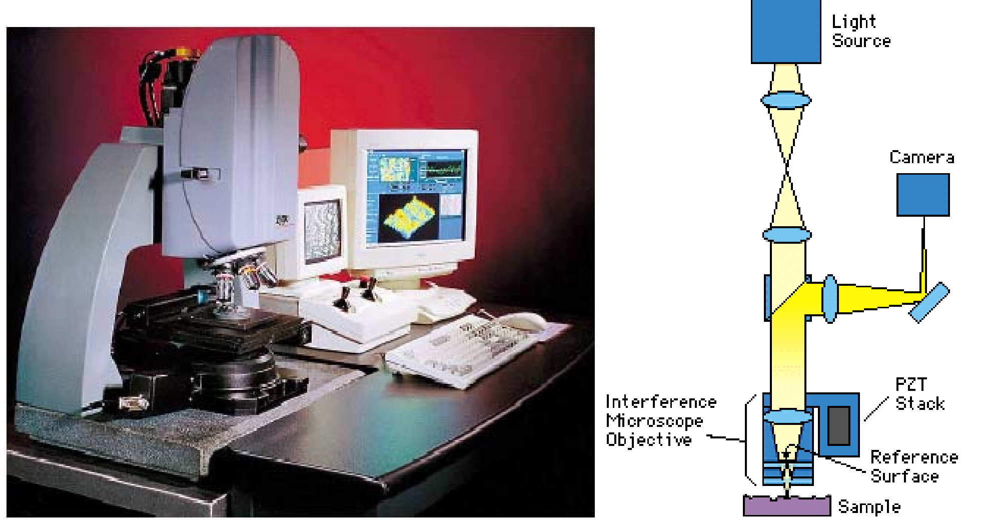

Figure 3.7: Picture of Zygo system and working schematic [21]

Interferometry is particularly useful in determining which beams in a buckling beam array have buckled and which have not. On each of the MUSiC-01 test chips, four fixed-fixed beam arrays were cast. Two sets of example beams are shown in Figure 3.8. These arrays are made up of a series of micro-bridges increasing in length from 110 µm to 900 µm in increments of 10 µm, each with a width of 10 µm. A cross-section file was not available for the L-edit program (a computer aided design program used to layout MEMS devices). However, from the labeling and design rules, the SiC-3 array should be 1.5-µm thick and the SiC-2 array should be 2.0-µm thick. This was to be a primary means of determining the residual stress of the SiC layers. This method relies upon the following equation for the maximum length before buckling occurs, which is based on Euler beam theory:

$$L = \sqrt{\frac{\pi^2 t^2 E}{3\sigma}} \quad (\mu m) \tag{3.4}$$

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Here, t (μm) is the beam thickness, σ (Pa) is the residual stress, and E (GPa) is the Young's modulus of the material. [4]

Figure 3.8 shows an L-edit image of these micro-beam arrays. Note how each array is labeled according to the layer it is cast in and numbers indicating the lengths of the beams.

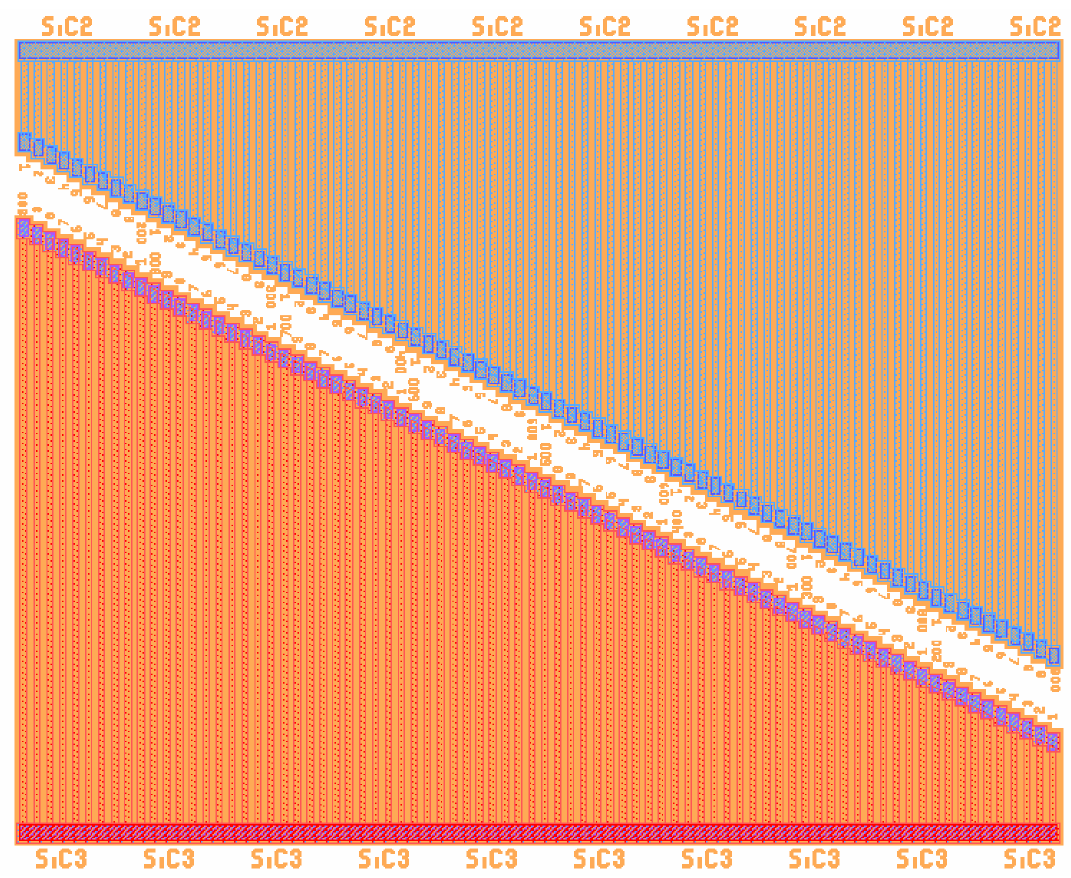

Figure 3.8: Fixed-fixed Euler buckling beam array [14]

3.5 Comb Drive ResonanceTtest

Young's modulus is a mechanical property most all solid materials possess and is defined as the slope of the stress-strain curve during elastic deformation. The elastic portion of the stress-strain curve is linear; hence, the relationship between stress and

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strain is a simple ratio which is called Young's modulus. The stiffer the material, the steeper the slope, and hence the larger the value for the Young's modulus where:

$$E = \frac{stress}{strain} = \frac{\sigma}{\varepsilon} \quad (\frac{N}{m^2}) \tag{3.5}$$

The hypothetical example curves in Figure 3.9 would be for a material that would undergo plastic deformation. SiC is not such a material; it is far too brittle. The curve for SiC will be a steep straight line almost all the way to the breaking point.

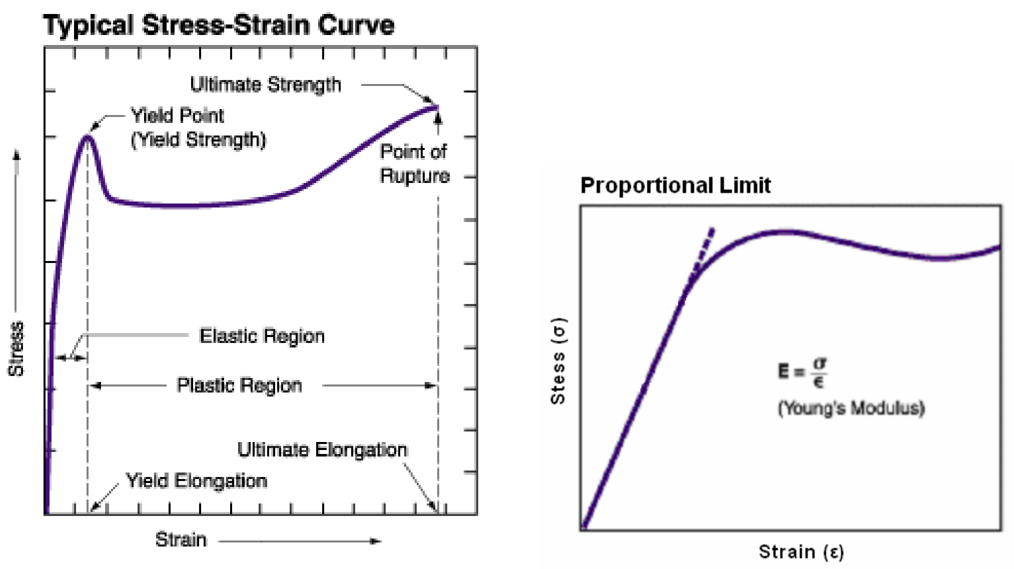

Figure 3.9: Example stress-strain curves in arbitrary units [22]

Young's modulus varies significantly according to slight and often uncontrollable changes in the fabrication process. Thus, it is advantageous to measure Young's modulus at a local level. Comb-drive resonators are a common device used to measure the Young's modulus of MEMS devices.[4] The AFIT test die for the MUSiC-01 run had

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two different comb drive designs, one for the SiC2 layer and the other for the SiC3 layer, as shown in Figure 3.10.

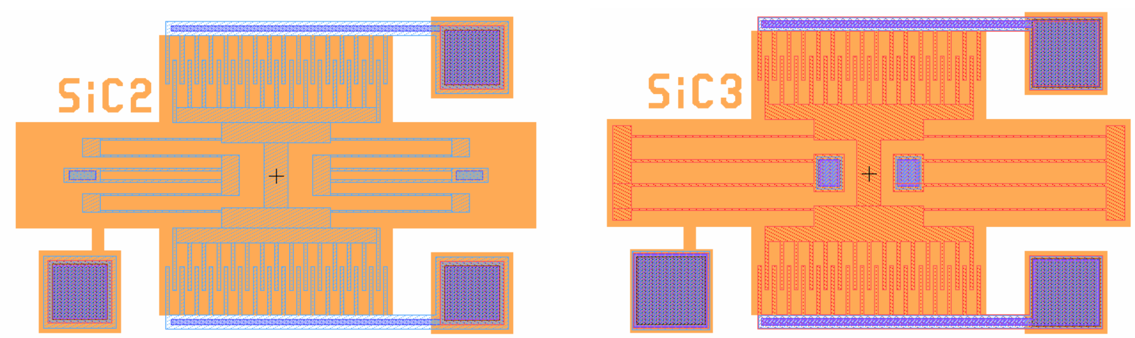

Figure 3.10: L-edit image of SiC2 and SiC3 comb drive lateral resonators [14]

Tang developed a mathematical model for the oscillating frequency of a comb drive. “Using the spring constant in the x-direction, k_x, the resonant frequency can be calculated as:

$$f = \frac{1}{2\pi}\sqrt{\frac{k_x}{M}} = \frac{1}{2\pi}\sqrt{\frac{24 E I_z}{\left(M_p + \frac{1}{4}M_t + \frac{12}{35}M_b\right)L^3}} \qquad (Hz) \qquad (3.6)$$

where E (Pa) is Young’s modulus, I_z (m^4) is the cross sectional moment of inertia for the beam with respect to the axis of rotation, L (μm) is the beam length, and M_p, M_t, and M_b are the masses of the plate, trusses and beams (kg), respectively.” [4] With this equation, a sinusoidal potential is used to induce a frequency response in the comb drive. When resonance is achieved (i.e., when the shuttle suddenly stops moving) the frequency is noted and Young’s modulus can then be calculated. A schematic of the test setup, provided by Dr. Starman, is shown in Figure 3.11. Setup and procedure directions are located in Appendix A.

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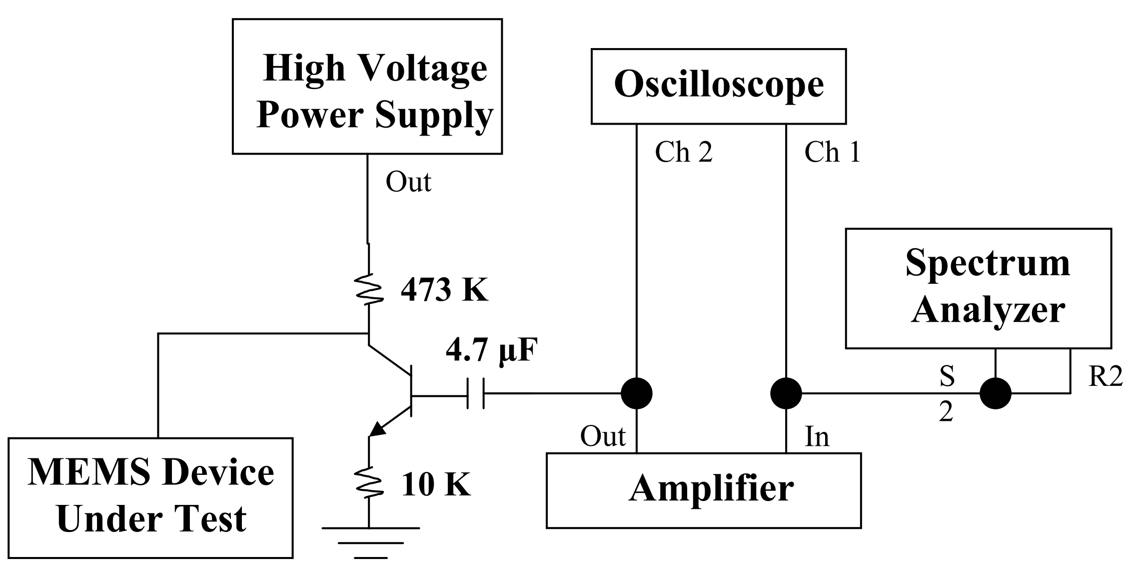

Figure 3.11: Test configuration for comb-drive resonance experiment [24]

Calculations for the approximate values for resonant frequency were performed using MathCAD and are located in Appendix C. For the SiC-2 comb drive, an estimated Young's modulus of 329 GPa [23] will give a resonant frequency of 58.6 kHz. The same modulus estimate will give a resonant frequency of 31.4 kHz for the SiC-3 comb drive. The difference in the two values is primarily due to the fact that the beams with the SiC-3 design are 50 µm longer. Therefore, the test range for SiC-2 will be from 55 kHz to 75 kHz, and the test range for SiC-3 will be from 25 kHz to 40 kHz.

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3.6 Conclusion

This thesis uses four different experiments to fully characterize the stress in SiC MEMS fabricated via the MUSiC^{SM} process. This chapter has described these experiments in detail, along with some background and theory on Raman spectroscopy. These experiments are Raman spectroscopy, release of MEMS via wet-chemical etching, interferometry measurements using a Zygo interferometer, and comb-drive resonance test.

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Chapter 4: Results and Analysis

This thesis conducted four different experiments, Raman spectroscopy, release of MEMS structures via wet chemical etching, comb-drive resonance frequency test, and interferometer surface mapping with a Zygo interferometer. Experiment setup and goals are outlined in the previous chapter, with the results and analysis given in this chapter.

4.1 Raman Spectra for Bulk SiC Samples

For the 4H-SiC sample, three scans at different locations on the samples were taken with the same scan parameters. Operating in a continuous extended mode from 2000 to -100 cm^{-1}, the 20x objective was used for 20 sec at 50% laser power (2.5 mW is full power). Figure 4.1 shows the average of these three scans.

This data agrees well with published Raman spectra of 4H-SiC (Figure 4.2). Notice in Figure 4.2 how some peaks increase in height as the excitation wavelength changes. The FLA peak shown in Figure 4.2 (around 610 cm^{-1}) is barely visible in the data take here (Figure 4.1), which was taken with a 514.5-nm excitation source.

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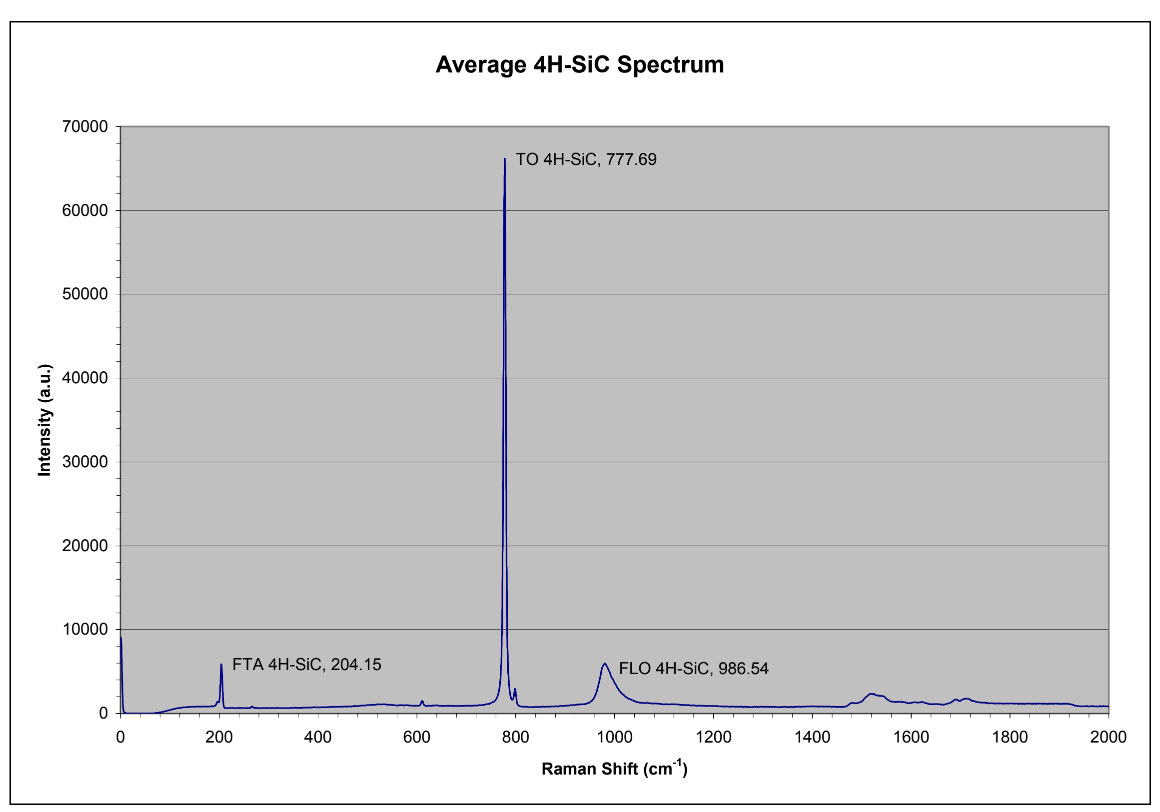

Figure 4.1: Average results of 4H-SiC micro-Raman spectra

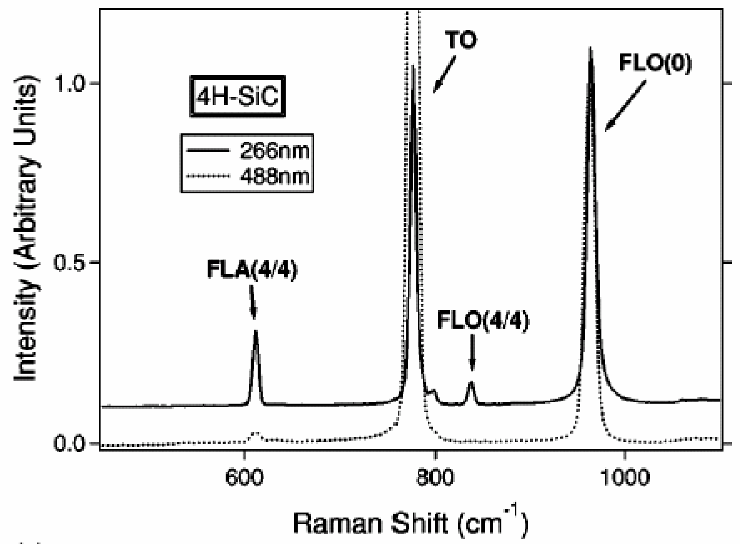

Figure 4.2: Reference Raman spectra for 4H-SiC for comparison to Fig. 4.1 [25]

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For the 6H-SiC sample, three scans at different locations on the samples were taken with the same scan parameters, except for laser power. The second and third scans were done at 50 % power because of saturation problems. Scans were done in a continuous extended mode from 2000 cm^{-1} to -100 cm^{-1} with the 20x objective for 10 sec. Figure 4.3 shows the spectra collected in this research and Figure 4.4 shows other published results for comparison.

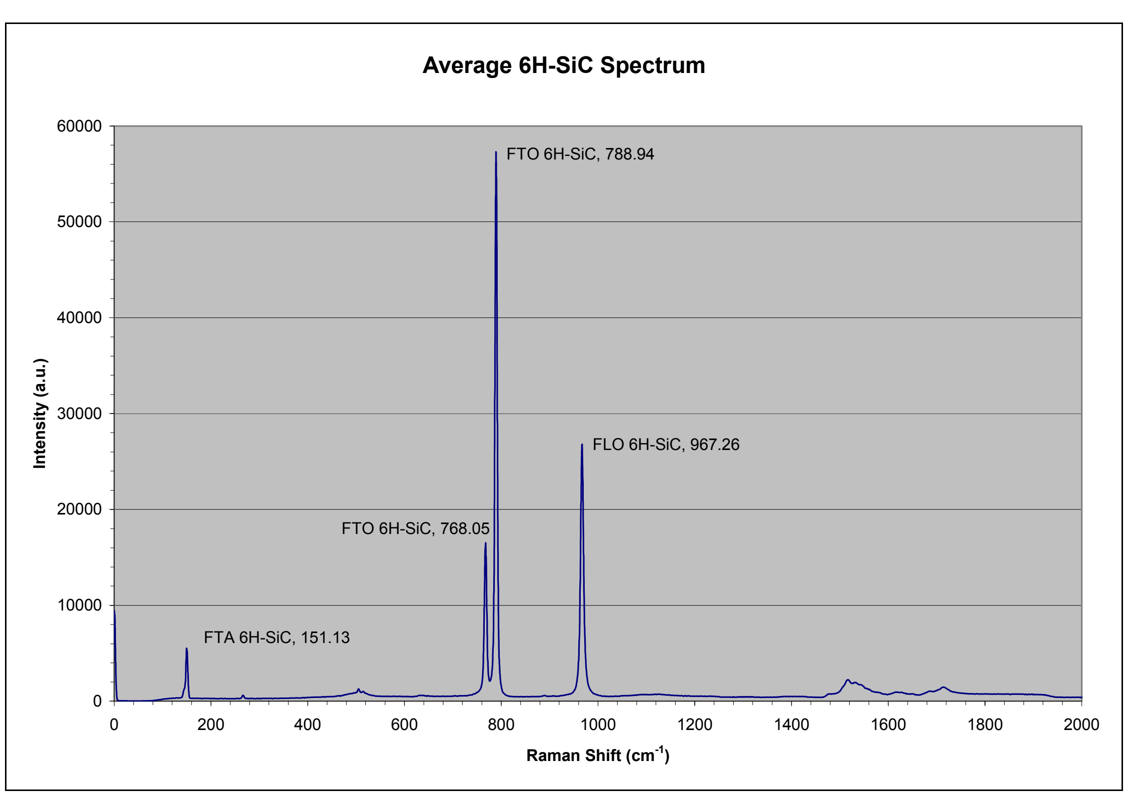

Figure 4.3: Average results of 6H-SiC Raman spectra

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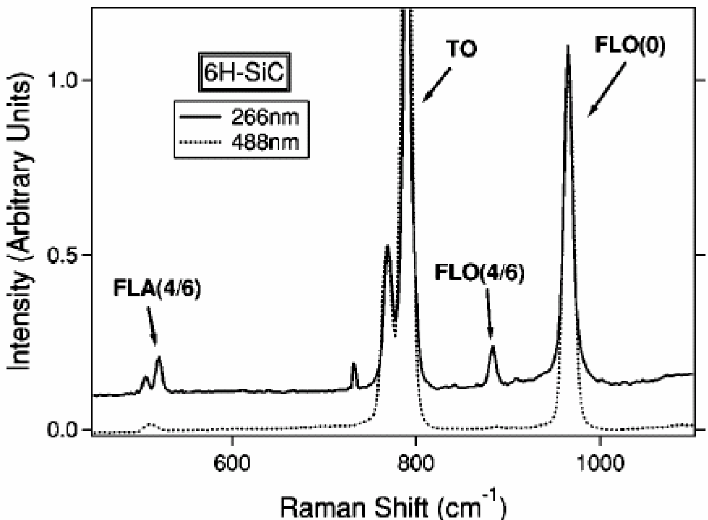

Figure 4.4: Reference Raman spectra for 6H-SiC for comparison with Figure 4.3 [25]

For the 15R-SiC sample, three scans at different locations on the samples were taken with the same scan parameters, except for laser power. The first scan was done at 50% power and the second and third scans were done at 100 % power (2.5 mW). Scans were done in a continuous extended mode from 2000 to -100 cm^{-1} with the 20x objective for 10 sec. Notice the increased number of peaks as crystalline structure becomes more complex. Figure 4.6 provides other published spectra for comparison.

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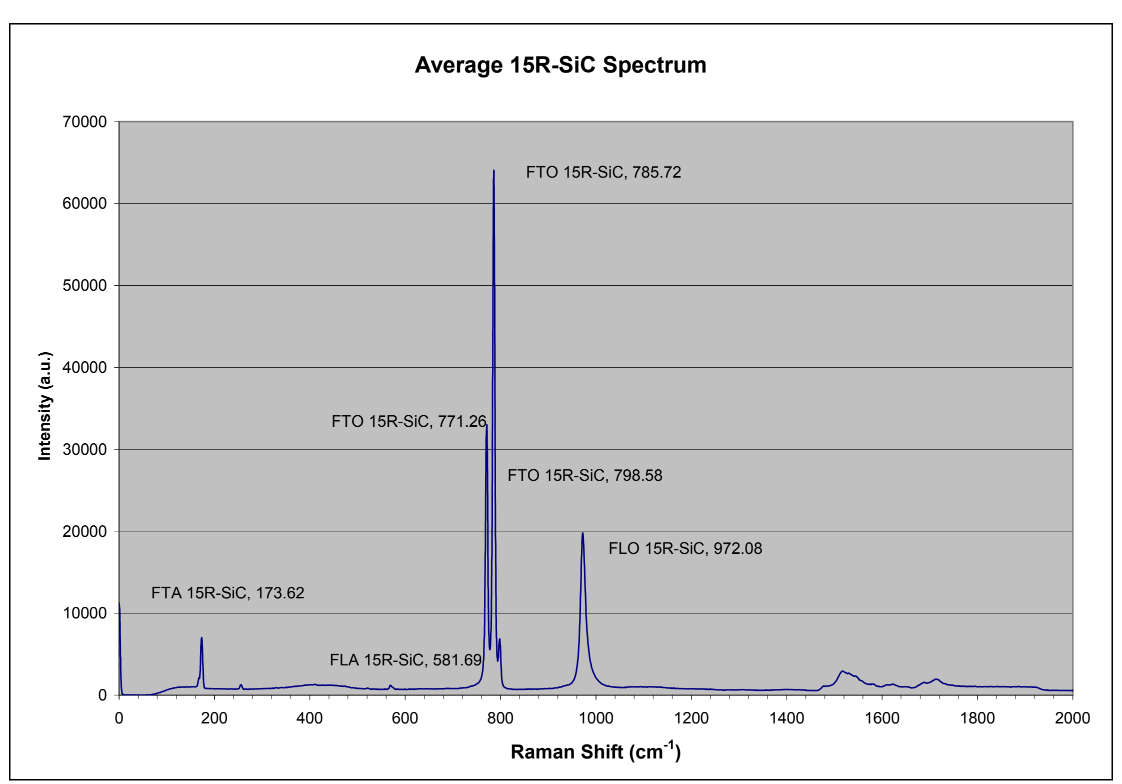

Figure 4.5: Average results of 15R-SiC Raman spectra

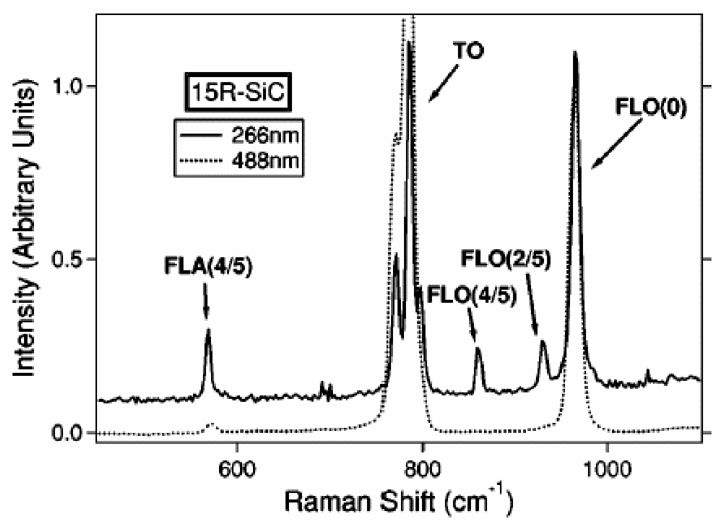

Figure 4.6: Reference Raman spectra for 15R-SiC for comparison with Figure 4.5 [25]

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A baseline spectra for 3C-SiC was also attempted by using a sample from FLX Micro, Inc. that had a 1 to 2-μm thick layer of PolySiC on a silicon wafer deposited by APCVD. Once again, three scans at three different locations where preformed with a 20x objective, for 20 sec at 100% power. The range was 1100 to -100 cm^{-1}. This did not produce very good results, as will be explained later. So, other samples were procured from FLX Micro, Inc. Four spectra (two from two chips) were collected with the 20x objective, from 1200 to –100 cm^{-1} at 100% power for 25 sec. The SiC on Si_3N_4 spectra was taken at 50% power for 20 sec. Figure 4.7 shows these results.

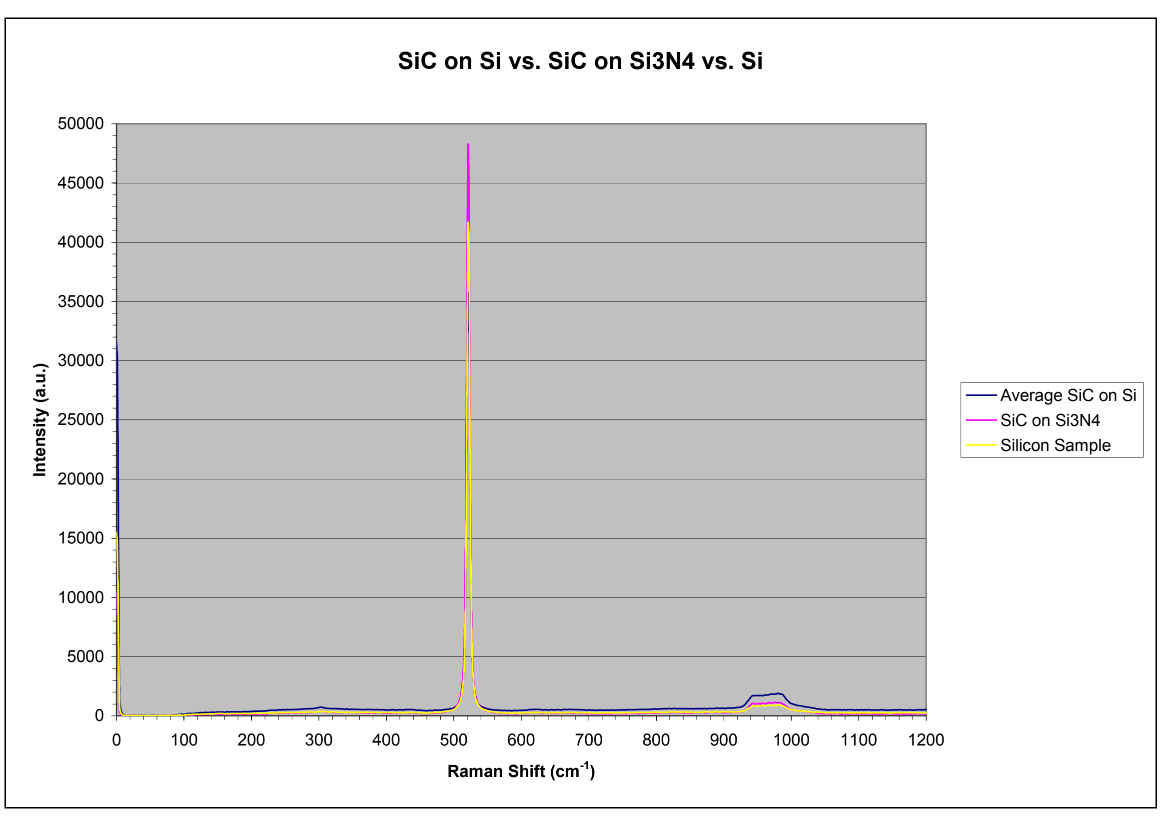

Figure 4.7: Results of 3C-SiC Raman spectra

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It is assumed that 3C-SiC is the dominant poly-type in PolySiC deposited by APCVD since it is first formed on a crystalline silicon wafer, which also has a cubic structure. However, the spectra collected in the Figure 4.7 are not what one would have expected, as is illustrated in Figure 4.8 with a FLO peak at 972 cm^{-1} and a FTO at 797 cm^{-1}. The spectra in Figure 4.7 indicate that the SiC poly-type on these samples is too transparent to the 514.5-nm wavelength radiation used to induce Raman scattering, or that the deposited 1- to 2-μm SiC film is too thin to scatter a useful Raman signal. Thus, baseline spectra for 3C-SiC was not obtained. Therefore, the published spectrum will be relied on for this thesis. The spectrum in Figure 4.8 was collected by A. J. Steckl and J. Devrajan, at the Nanoelectronic Laboratory, University of Cincinnati, from a crystal of 3C-SiC grown via methyltrichlorosilane.

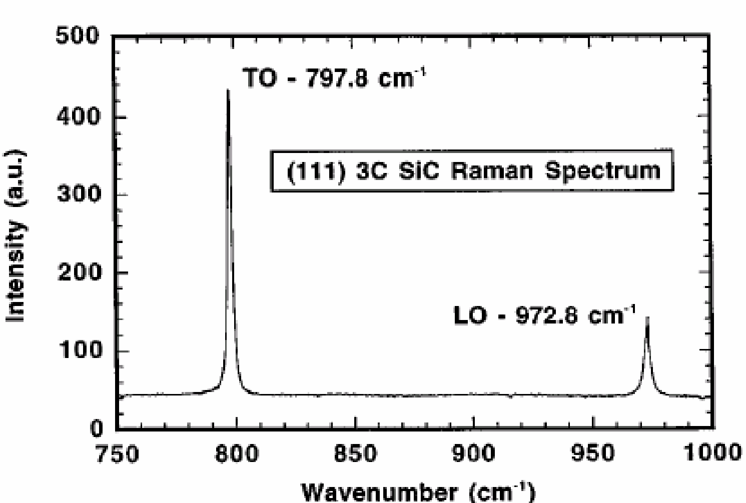

Figure 4.8: Raman spectrum taken in the backscattering configuration from the (111) surface of the 3C-SiC crystal shown in Figure 4.9 at 300K [26]

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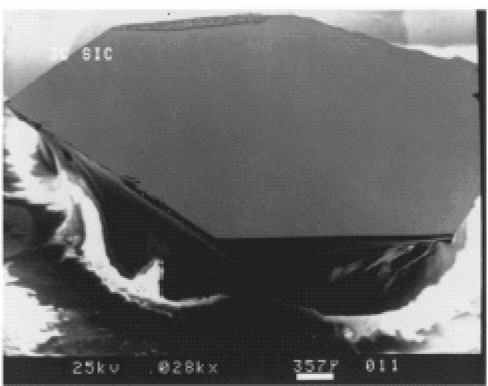

Figure 4.9: Photograph of undoped 3C-SiC grown by methyltrichlorosilane [26]

4.2 MUSiC-01 Raman Spectra

In early December 2002, the first MUSiC^{SM} run was complete, and data collected from several locations noted in Figure 4.10. It was anticipated that a useful Raman spectrum would be obtainable from locations on the chips with the thickest SiC. The chips themselves were very inconsistent as a finished product, which was to be somewhat expected as a first run of a new process. As indicated in Figure 4.10, these points (1-9) were scanned to test the quality of spectra available from these samples before moving on to beams and cantilevers to obtain stress distributions. Points 1-7 are anchor points for some Guckel rings of about 6-µm thickness. Point 8 is an anchor for some test gauges and point 9 is on a beam of one of these gauges. These were taken with a 50x objective lens from 1200 to -100 cm^{-1} for 60 seconds in an extended continuous mode at 100% (2.5 mW) power. The results are shown in Figure 4.11.

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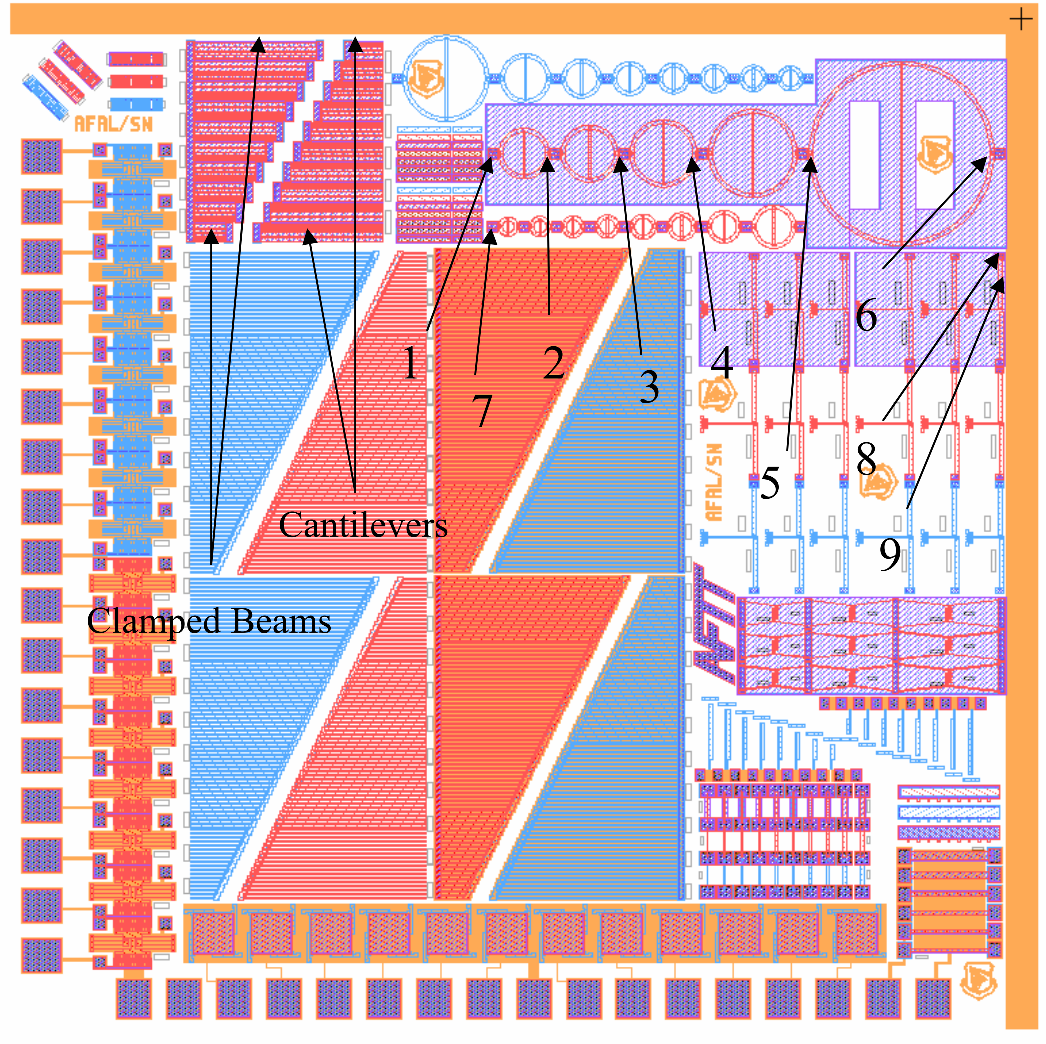

Figure 4.10: Pre-release Raman scan locations [14]

Getting sharp spectral lines are very important in order to determine the relative Raman shift from point to point across a beam, and thus a profile of the residual stress in the material. After collecting these spectra, it was apparent that getting the desired quality in spectra would be hampered by problems in three critical areas of Raman spectroscopy: florescence, penetration depth, and line broadening. In Figure 4.11, notice the sharp decline at the lower wavenumbers from 0 to 150 cm^{-1}. This is caused by the

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rejection filter that reduces the laser line at the CCD. More importantly, it indicates the base intensity is very high and can be observed to increase on a constant slope as wavenumbers increase. This is a classic indication of fluorescence.

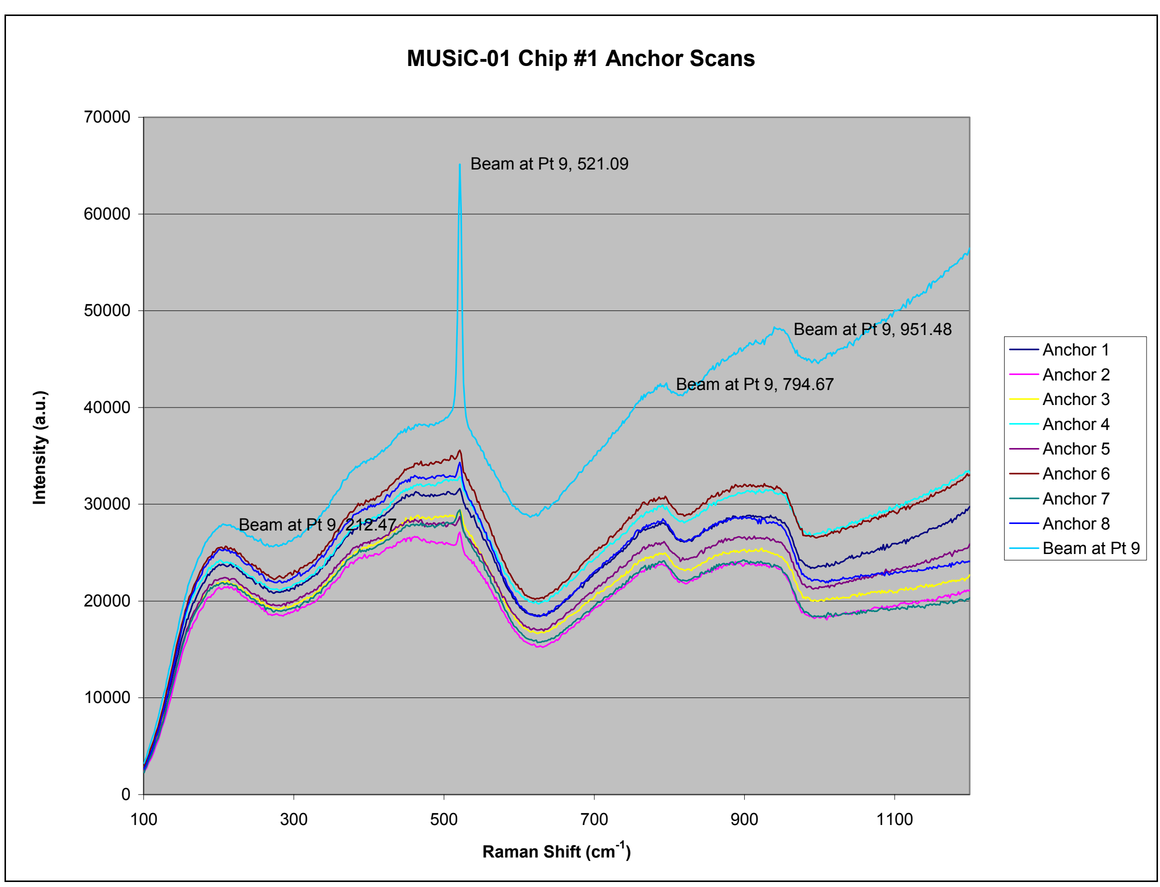

Figure 4.11: Raman anchor scans for MUSiC-01 chip #1

The presence of a sharp silicon peak at 520 cm^{-1}, which is more pronounced on the thin beam, indicates the Raman scattering being collected is off the silicon substrate and not from the thin SiC layers. The problem here is lack of absorption and, hence, too large of a penetration depth at the 514.5-nm wavelength. Therefore, even though the

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films on the finished MEMS chips are thicker than the bulk samples, a penetration problem will still exists.

Again, a FLO peak at 972 cm^{-1} and a FTO at 796 cm^{-1} was expected for a sample that is mostly 3C-SiC. Instead, broad peaks were observed in roughly those locations. The peak around 794.67 cm^{-1} in the data is somewhat more reliable to accept as a 3C-SiC peak; not so with the peak at 951.48 cm^{-1}. Silicon also had second order peaks around that location from 930 cm^{-1} to 1000 cm^{-1}, and the broadening could also be attributed to the presence of other SiC poly-types. Notice a broadening of the peaks in Figure 4.12 when the 4H-, 6H-, and 15R-SiC baseline spectra are averaged together.

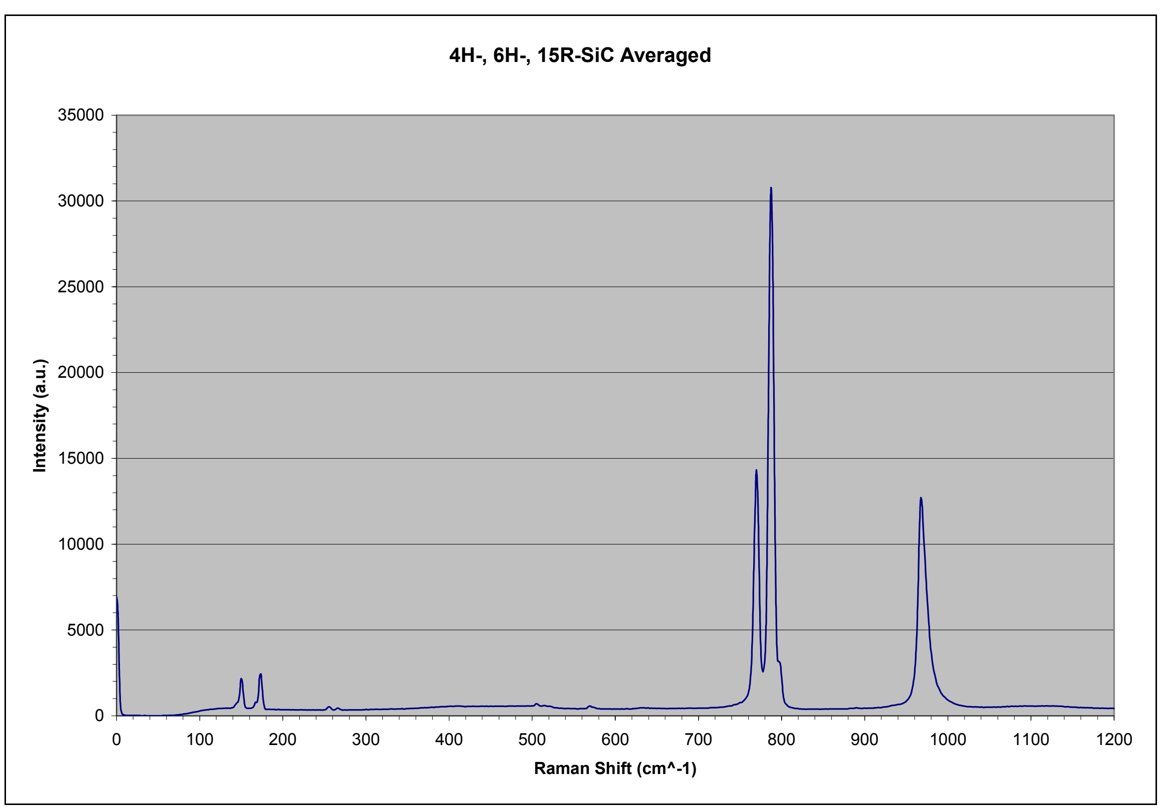

Figure 4.12: 4H-, 6H-, 15R-SiC averaged Raman spectra

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4.3 Release Experiments

Four chips were released overall, and all reactions took place at room temperature in a cleanroom environment. To illustrate the results, each release session's procedure is put forth in the following sections to include post-etched pictures and the rationale for each step in the process.

4.3.1 07 January 2003

This procedure etched the same two chips from which pre-release Raman spectra were collected. Both chips were etched at the same time, being moved from one beaker to the next with cleanroom grade tweezers. Several beakers were set-up under the ventilation hood for the following etching dips:

1. Acetone
2. 5 (HNO_3):3 (HF):3 (CH_3COOH) (total of 110 ml)
3. Methanol
4. Methanol

Here is the procedure with times included.

1. 15 min in beaker 1 (acetone) to remove any photo resist that might be on the chips.

2. 2 min in acid etching solution—originally planned to start with only one minute first then examine under a microscope, but changed plan since the acid solution would not etch the SiC in any significant manner, and to save time, they were etched for two minutes. Mild agitation of the beaker occurred during the etching.

3. 5 min in beaker 3 methanol to rinse

4. 5 min in beaker 4 methanol to rinse

5. Both chips examined under microscope. At this point, the chips were taken out of the methanol, and of course the methanol evaporated from the surface of the chip rather quickly. Chip #1 had quite a bit of damage to the structures, but looked completely etched. Chip #2 looked well-etched in some areas but had a reddish-brown material around a great majority of the structures. The

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reddish-brown material seemed to indicate that the chips needed more etching. So, both chips were etched in the following manner.

6. 3 min in beaker 2 acid etch

7. 5 min in beaker 3 of methanol to rinse

8. 5 min in beaker 3 of methanol to rinse

9. Examined under microscope again, and found the reddish-brown material to still be present on chip #2 and more extensive damage to the structures on chip #1. The procedure concluded at this point, since the reddish-brown film did not etch.

10. Hot-plate dry at 100° C for 1 min.

Figures 4.13 and 4.14 contain pictures under x10 microscope objective of both chips after release.

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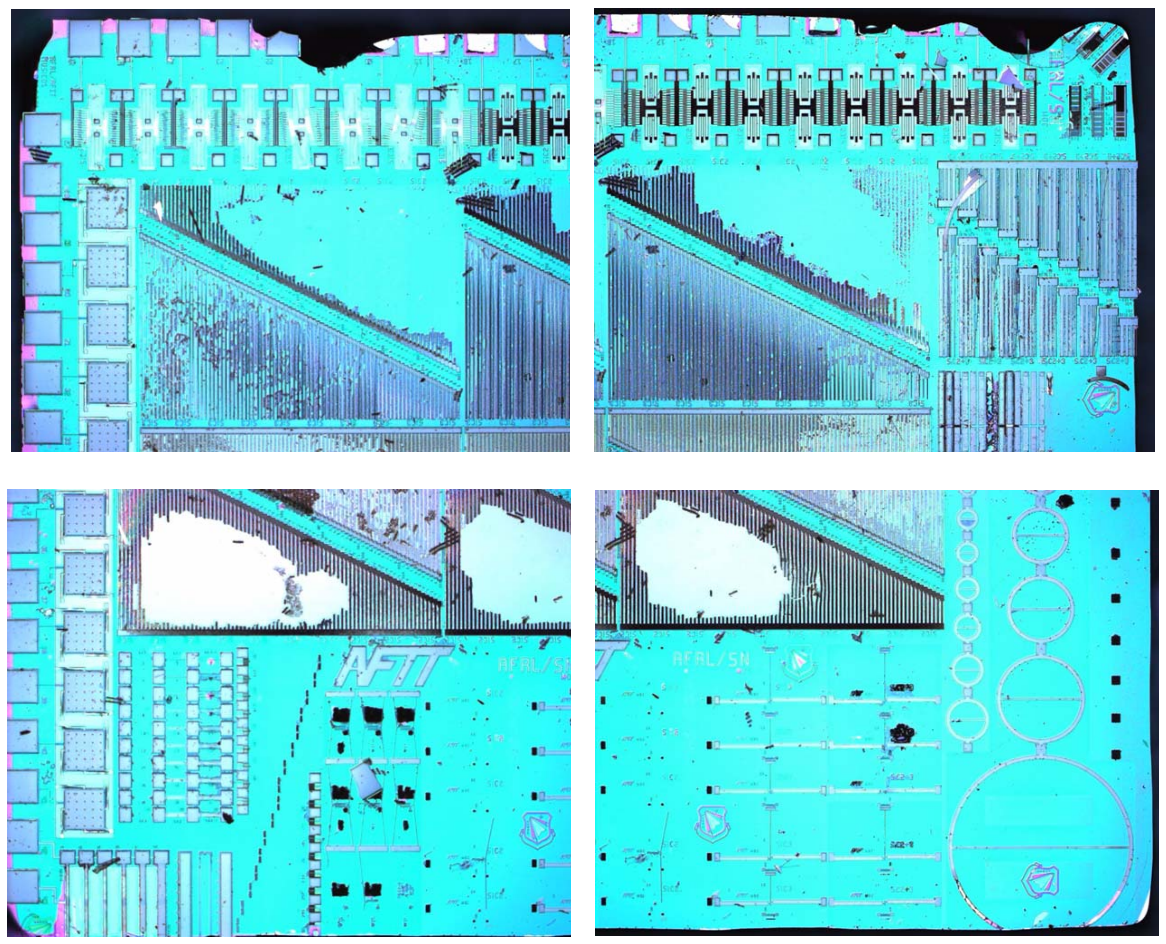

Figure 4.13: Post-Etch MUSiC-01 Chip #1

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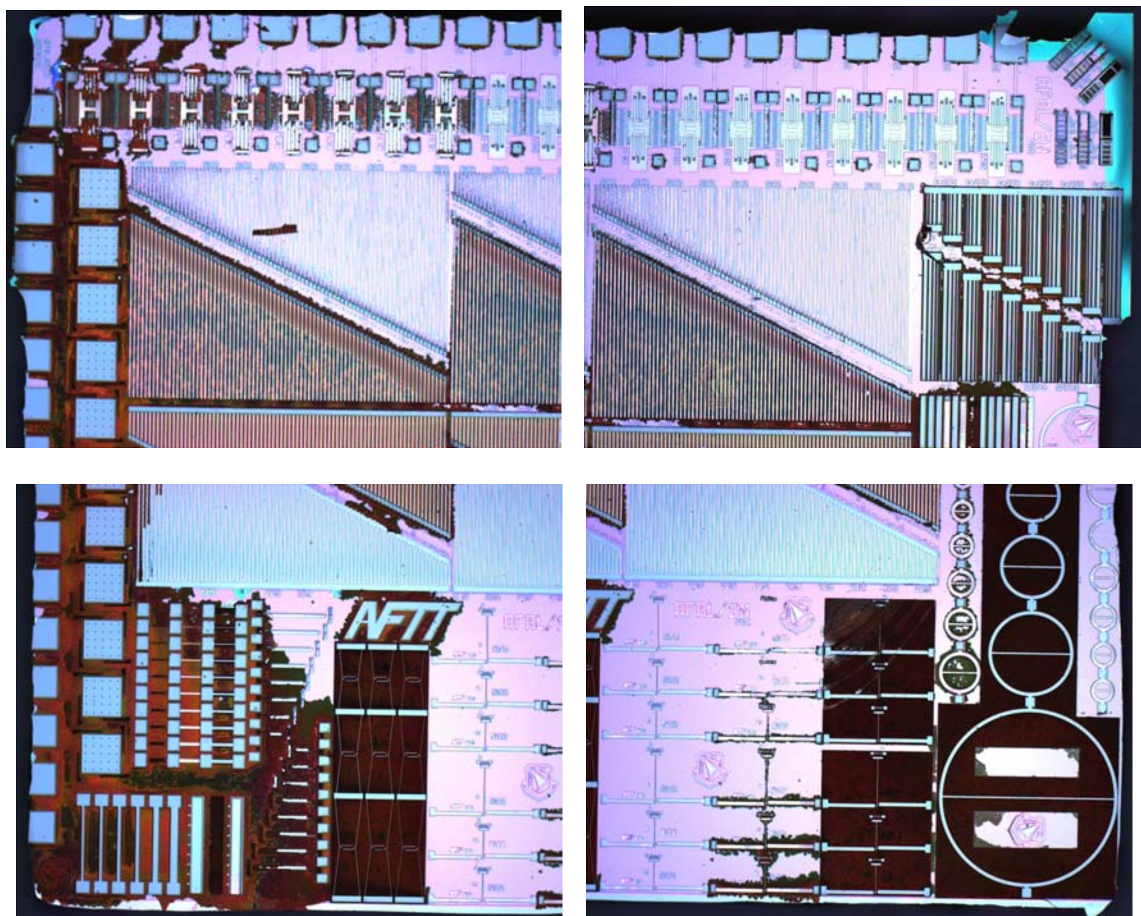

Figure 4.14: Post-Etch MUSiC-01 Chip #2

4.3.2 15 January 2003

This procedure etched an additional chip from the MUSiC-01 run. This chip was moved from one beaker to the next with cleanroom-grade tweezers. Several beakers were setup under the ventilation hood for etching dips. The procedure to etch the MUSiC-01 chip #3 is as follows:

1. Mix KOH solution:
    a. Filled 50 ml of DI H_2O in a 250 ml beaker
    b. Cover beaker and place on hotplate set to 140° C

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   c. Weigh out 0.42 g of dry KOH pellets
   d. Place KOH pellets in 50 ml of heated H_2O (does not have to reach 140° C)
2. Placed chip in acetone solution for 15 min
3. Placed chip in 48% HF solution for 1 min
4. Placed chip in KOH solution for 40 min or until bubbling almost completely stops
5. Place chip in 48% HF solution for 10 min
6. Rinse in methanol for 5 min
7. Rinse in methanol for 5 min
8. Dry with supercritical CO_2 dryer

This was done without any guidance on time tables or KOH concentration, and it was discovered after the procedure that there were not enough KOH pellets in stock to mix up a solution that would make a strong enough concentration. This drove the need to etch this chip again on 04 Feb 03 with a stronger solution of KOH (9 g KOH pellets/20 ml H_2O). "In general, concentrations below 20 wt% are not used due to high surface roughness and the formation of potential insoluble precipitates. A more typical concentration of KOH is in the range of 40 wt%." [7] Figure 4.15 shows the chips after the first etching described above.

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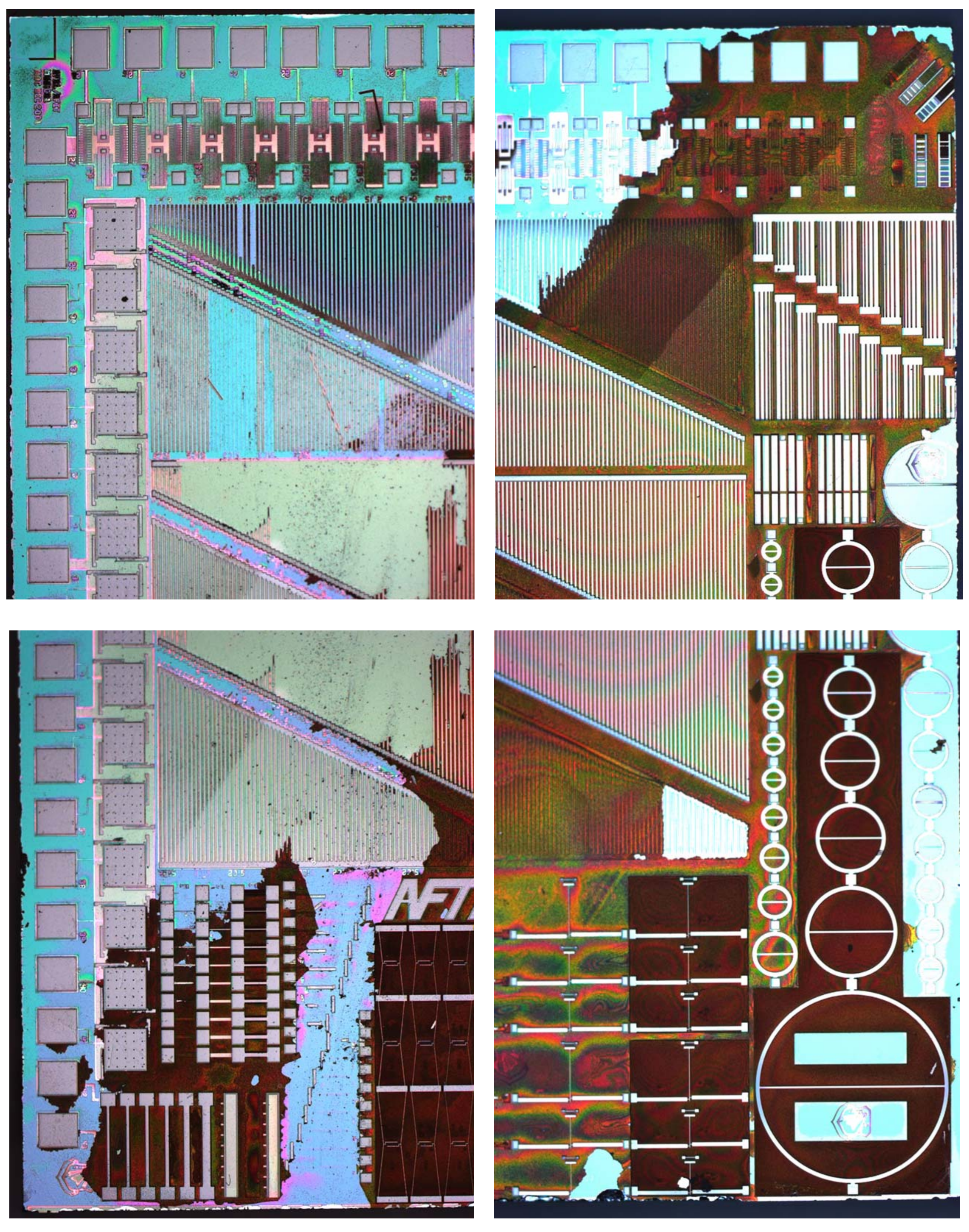

Figure 4.15: Post-etch MUSiC-01 Chip #3

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4.3.3 04 February 2003

To get a released chip with a high yield of testable structures, a fourth chip was etched on this day. The guidance given from FLX Micro, Inc. as presented in Appendix B was followed for this procedure. Also, the chips were placed in a clamp to minimize the possibility of damaging the structures from handling them with tweezers or excessive agitation while in the etching fluids. Figure 4.16 shows the end result, and the procedure was as follows:

1. Lock chip in clamping holder
2. 15 min in acetone
3. 3.5 min in 48% HF
4. 10 min in 45% KOH (9 g KOH pellets/20 ml H_2O)
5. 8 min in 48% HF
6. 10 min in methanol
7. Remove from clamp and placed in basket for CO_2 dry

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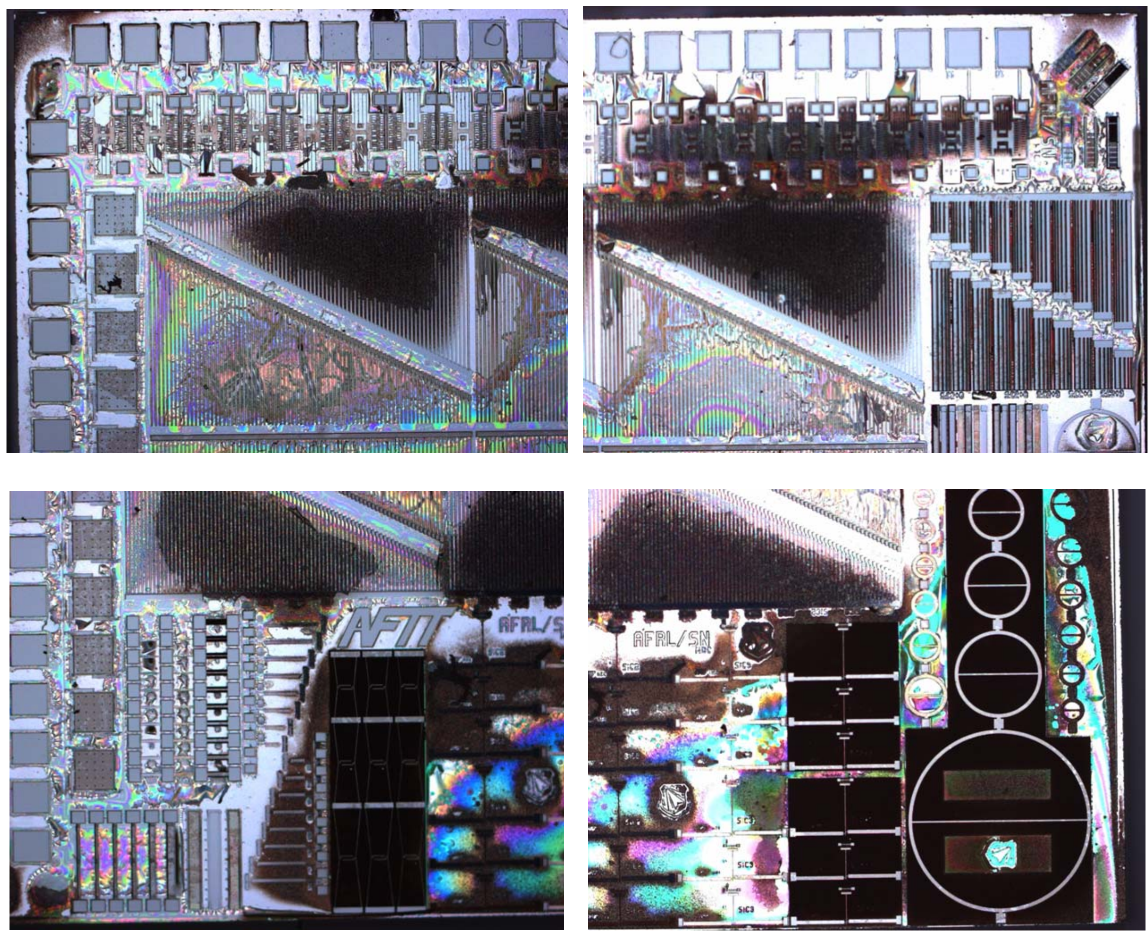

Figure 4.16: Post-Etch MUSiC-01 Chip #4

As stated before, clear guidance was not given before the procedure, so the process whereby KOH etches silicon was not understood. It is possible that the reaction was slowed due to an increasing concentration of KOH, lack of available H_2O in solution and low solution temperature. So, not only is there a problem with residual SiC (reddish-brown film), Chip #4 may also have polysilicon left on the chip, which appears as shiny iridescent material in between the structures. An important point to observe in Figure 4.16 is the lack of damage to the structures that one can see on the other chips. This can

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be attributed to the use of a clamping stick that Chip #4 was placed in during etching and the use of the supercritical CO_2 dryer. Another noteworthy observation was an audible reaction during the etching process when the chip was placed in KOH after having been in HF. Rinsing in de-ionized (DI) water between the HF and KOH beakers should eliminate this problem and the potential source of damage.

Chip #3 was etched again on this day in a stronger KOH solution with the goal of ensuring a full release. Figure 4.17 shows the end result, and the procedure was as follows:

1. 1 min 48% HF
2. 10 min in 45% KOH
3. 8 min in 48 % HF
4. 10 min in methanol
5. Placed in basket for CO_2 dry

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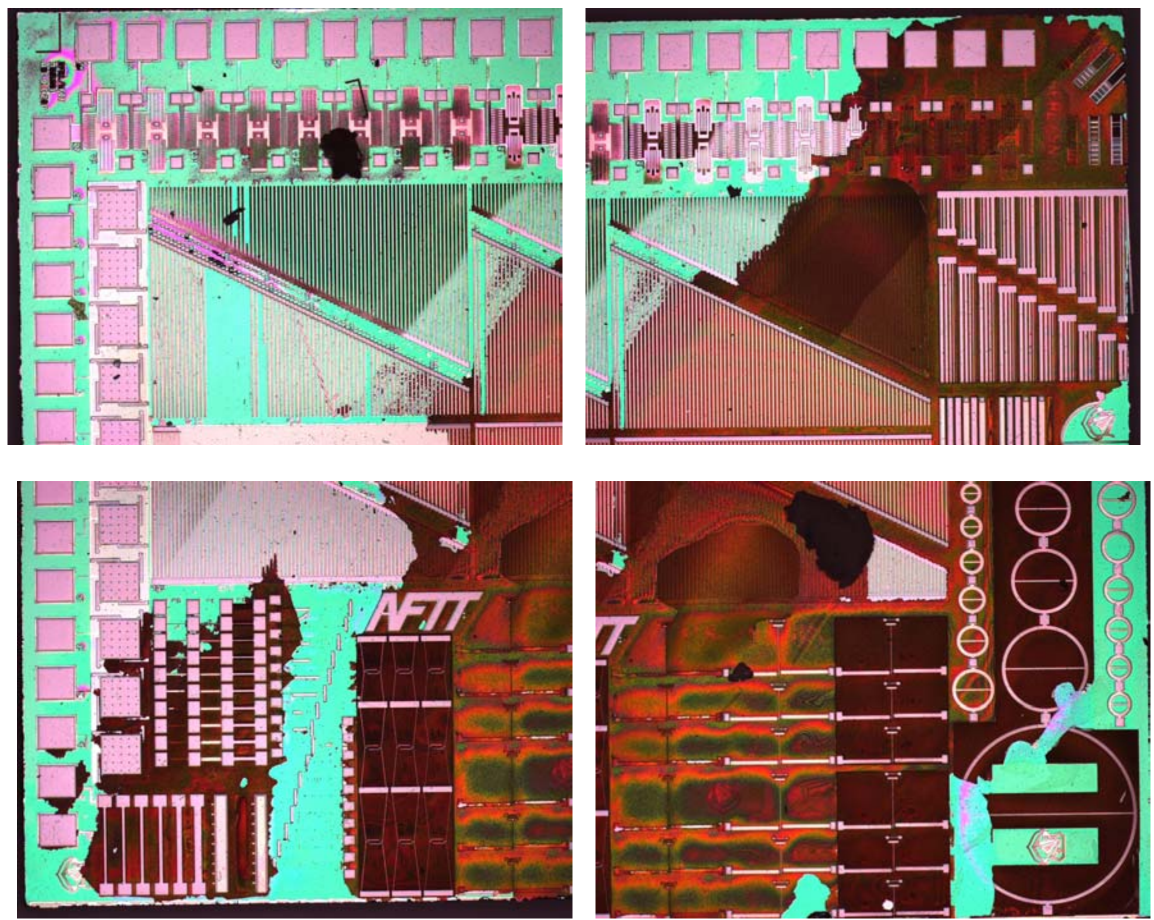

Figure 4.17: Post-etch MUSiC-01 Chip #3 after second etching

This did not seem to produce much change except for some to the reddish-brown film coming off and taking part of the largest Guckel ring with it.

After etching, some of the structures were probed to see how well they were released. On all four chips, even on Chip #1 that was etched for a great deal longer than it needed to be, the SiC-2 comb drives were either stuck down or not released, while the SiC-3 comb drives moved freely when probed. It is possible that the SiC-2 layer was not completely leveled with the mold via CMP. A thin film of PolySiC remained covering the SiC-2 mold of PolySi, thus prohibiting it from being etched, and the SiC-2 and SiC-1

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layers from being released. The other possibility is simply that the SiC-2 comb drives were stuck down to the substrate.

4.4 Zygo Interferometry

All four released chips were inspected with the Zygo interferometer. With such a high degree of variation in the quality and yield of the MEMS structures, there was no systematic way of inspecting these chips. In addition, very few produced any results. Chip #1 had a great deal of damage to the structures, but yielded some good pictures that provide some indication of the stress, particularly in the SiC-3 layer. Figure 4.18 shows a SiC-3 buckling beam array with all but eight of the shorter beams buckled. With beams 1-7 and 9 unbuckled, one can calculate the stress of the SiC-3 layer with an estimated value of 329 GPa [22] for Young's Modulus (E) and the following equation.

$$L = \sqrt{\frac{\pi^2 t^2 E}{3\sigma}} \quad (\mu m) \qquad (3.4)$$

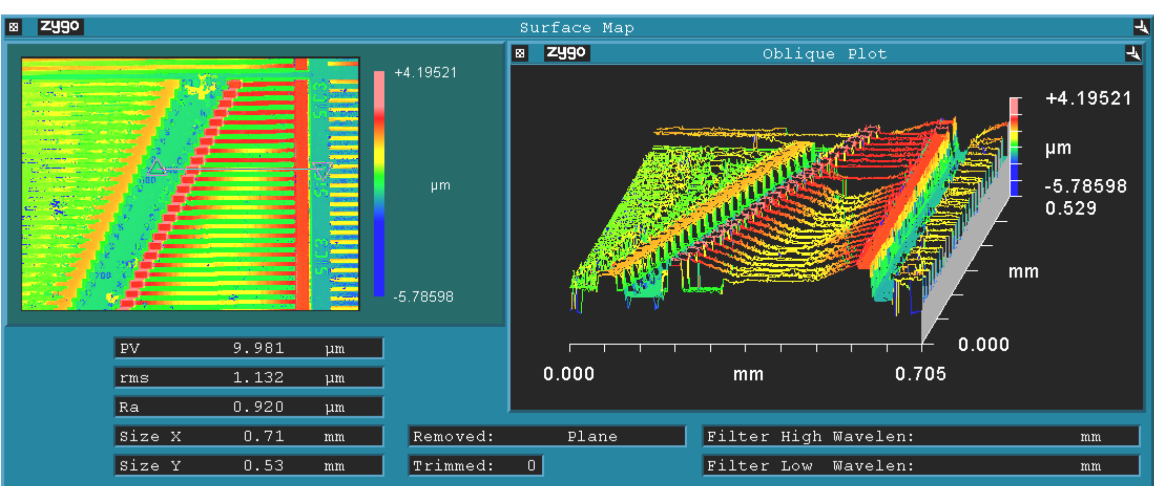

Figure 4.18: SiC-3 fixed-fixed beam array on chip #1 with eight beams unbuckled

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These calculations were accomplished with MathCAD and are given in Appendix C. From Figure 4.18, the stress could be estimated to be between 67 MPa and 84 MPa. However, this is only one data point; more would provide a better value for the general stress in the SiC-3 layer. Notice the difference in Figure 4.19, which is the other SiC-3 fixed-fixed beam array on Chip #1 in which all of the beams have buckled, which indicates the stress might be over 201 MPa.

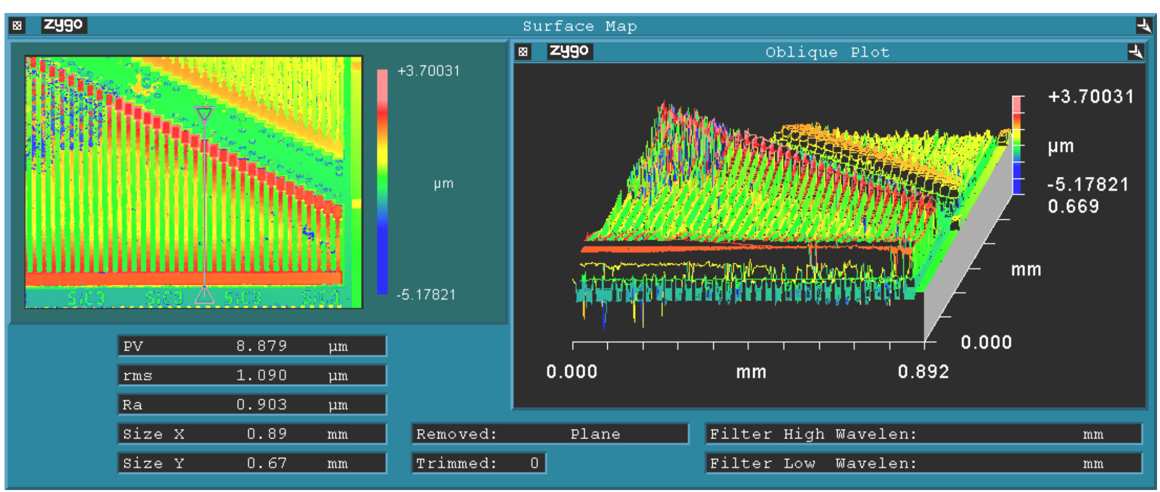

Figure 4.19: SiC-3 fixed-fixed beam array on chip #1 will all beams buckled

On the other hand, the possibility exists that these structures are stuck down, rendering this data meaningless. In order to be sure of the stress measured from this method, two things would need to happen. First, a localized modulus measurement of the material is required via comb-drive resonance or some other method. And second, several viable beam arrays should be released and the results from each statistically averaged.

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From Chip #1, Figure 4.20 is a good demonstration of the random stress distribution that exists in these devices. These arrays have beams and bridges that are 4-, 8-, 16-, and 20-μm wide with lengths from 150 to 600 μm in 50-μm increments. Notice how some cantilevers are bent up and others bent down with some variation and some consistent trends. The widest beams (20 μm) are all completely flat; this indicates that they are not fully released. Some of the next widest beams are partially released and the tips are curling up, indicating the presences of residual stress. The three narrower beams appear to all be released, several of which seem to be stuck down to the substrate.

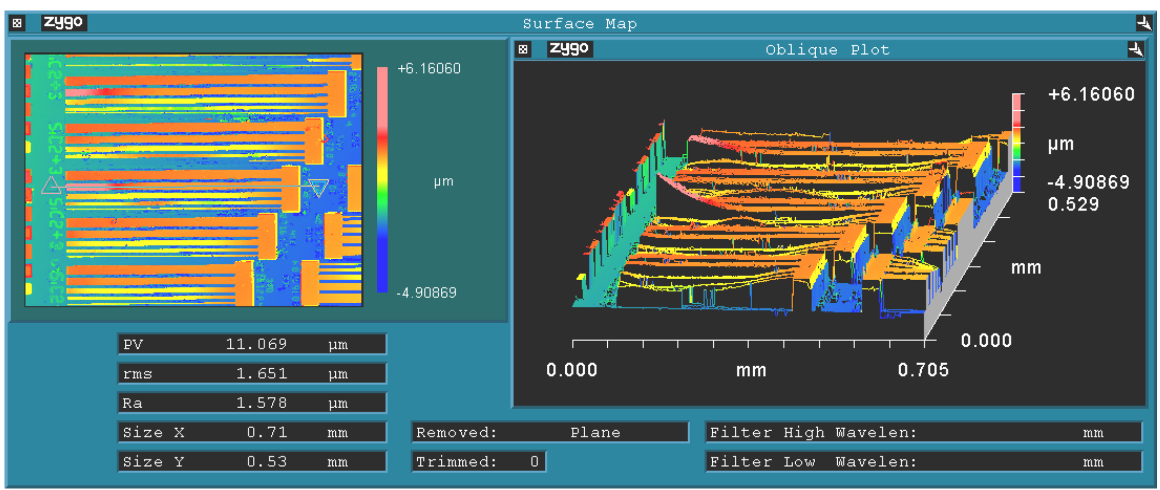

Figure 4.20: SiC-2+3 cantilever arrays on Chip #1

For Chip #2, the SiC-3 beams were too surrounded or covered with the reddish-brown film to get any good surface scans with the interferometer. Notice in Figure 4.21 that the reddish-brown film appears as low blue areas around the cantilever array and that the cantilevers are stuck down to the substrate.

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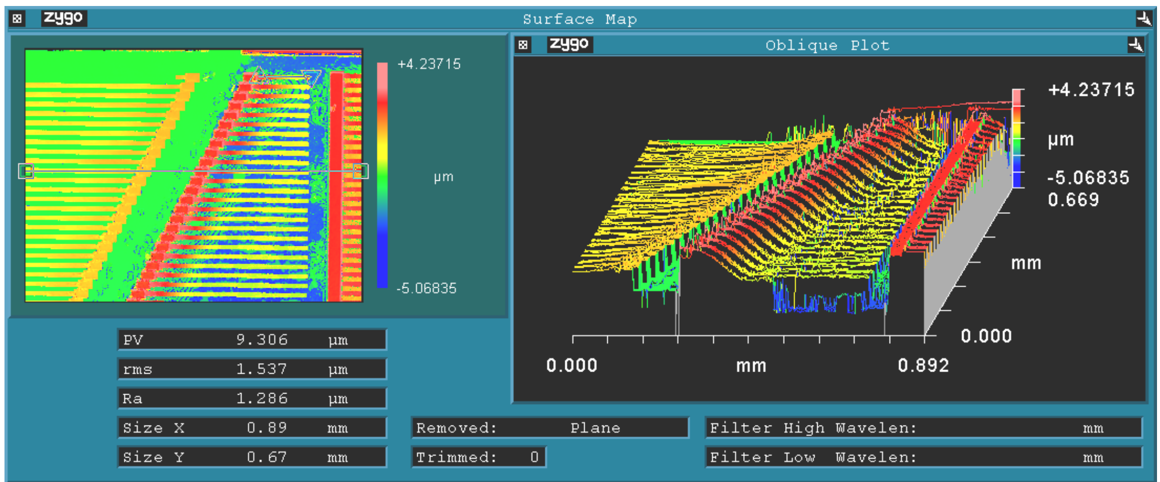

Figure 4.21: SiC-3 cantilever arrays on Chip #2

Figure 4.22 illustrates how the SiC-2 layer is not fully released (i.e., stuck to SiC-1 layer). Notice the cantilever array at the bottom of the picture that is the SiC-2 layer; they are completely flat. If the cantilevers were fully released, it is expected that they would curl, as well.

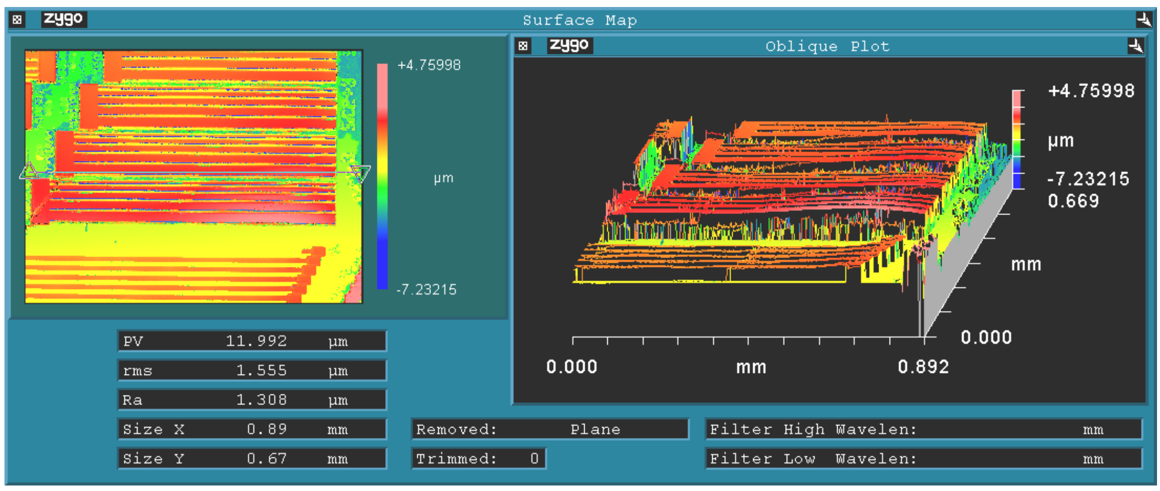

Figure 4.22: Cantilever arrays on chip #2

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Chip #3 not only had a lot of damage, but also a large amount of the reddish-brown film. But, Figure 4.23 shows some cantilevers from that chip that are uniformly curling up. These cantilevers were cast in the SiC-3 layer and show that there is a compressive residual stress at the bottom of the layer before release. Thus, upon release they bow upward. Since this is the SiC-3 layer (etched by RIE), there should be no residual stress in the top of this layer.

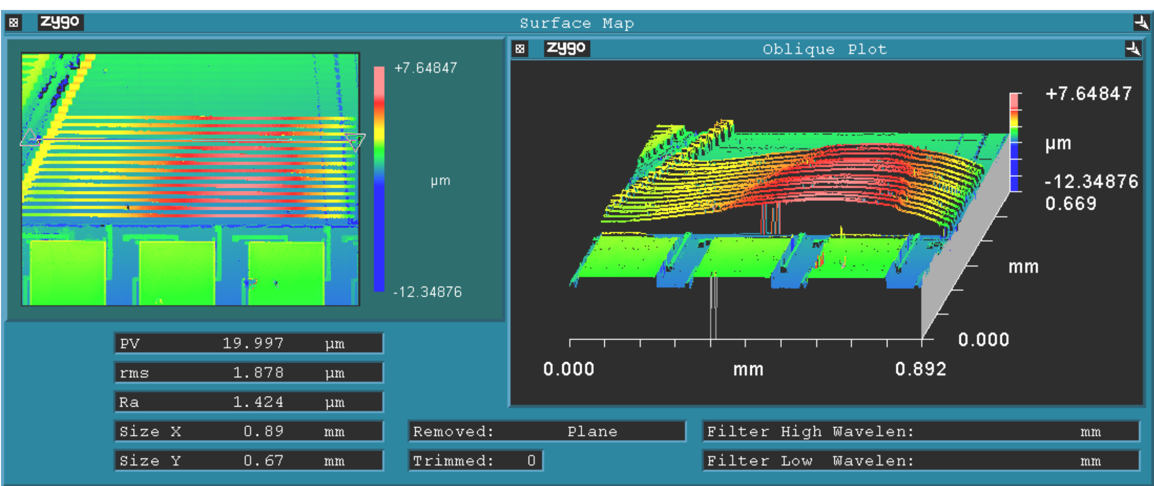

Figure 4.23: Remaining portion of a SiC-3 cantilever array on chip #3

Chip #4 had a thin film of semi-transparent material (most likely PolySi) deposited in between the structures. This material induced too much interference with the fringe patterns to get any surface scans with the interferometer. This film can be seen in Figure 4.16 and appears iridescent in nature.

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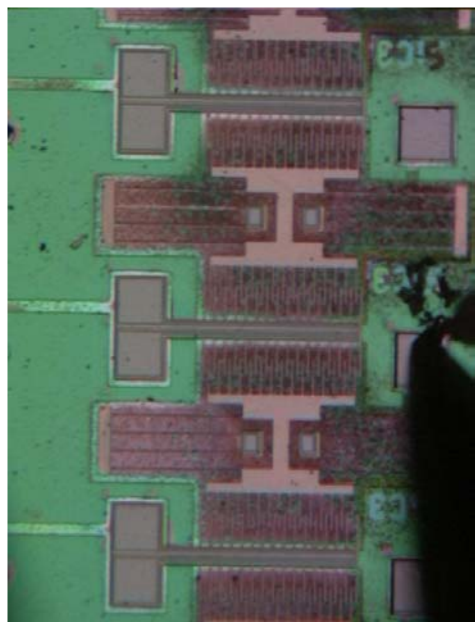
4.5 Comb Drive Resonance Test

To measure the Young's modulus of the MUSiC-01 chips, a comb-drive resonance test was performed. Section 3.5 describes the background and theory for this test. The MEMS chips were placed on a probe station with a microscope. Two probes were used, one as the ground and the other as the input to the 'MEMS device under test' as shown in Appendix A. In Figure 4.24, these probes can be seen touching the nickel bond pad at the edges of the photographs. At first, many of the SiC-2 layer comb drives looked in great shape to perform the test. But upon probing, it became clear that they were either not completely released or stuck down to the substrate and, therefore, unable to move. Looking at Figure 4.21 and 4.22, it appears that some of the SiC-2 beams (orange in color) are stuck down to the substrate, which indicates the SiC-2 comb-drives are, as well. The SiC-3 comb drives were released and, with a slight tap with the probe, shuttle movement and beam flexure could be observed.



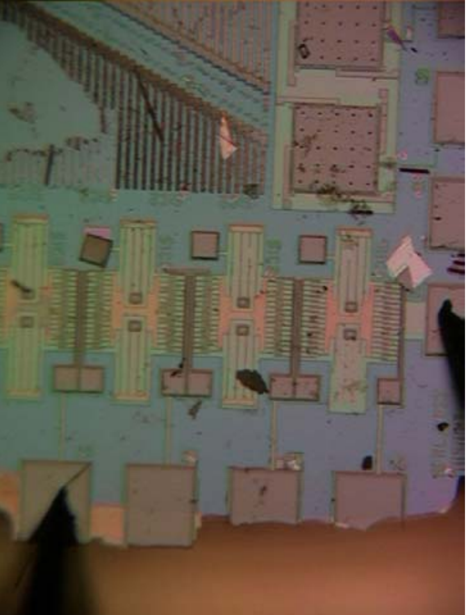


Figure 4.24: SiC-3 comb drives under resonance test

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After the test was all set up, voltage was applied but no visible actuation of the SiC-3 comb drive occurred. Next, a DC voltage of 500 V was applied to see if the shuttle would simply move, but there was no movement at all.

4.6 Conclusion

The results of the experiments were in general somewhat limited in quantity and in some cases quality. This was due primarily to the poor quality of sample from the MUSiC-01 run. As mentioned before, this was the first MUSiC^{SM} run and future samples should be of a much higher quality. Therefore, the Raman spectra for the bulk samples were the best results collected and completely filled requirements. The Raman spectra collected from the MUSiC-01 samples were not useful in determining the residual stress as intended for this thesis, but they do serve to point future work in the right direction. The release procedures also give guidance on better ways to release SiC MEMS. The IFM results did not provide the intended data due to the poor quality of the samples, and the comb-drive resonance test simply failed to provide any useful data.

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Chapter 5: Recommendation and Future Work

This chapter reviews the results of each experiment conducted during the research and provides any conclusions that might be drawn. Lessons learned are presented and future work is recommended for the remaining four test chips and any future test chips.

5.1 Raman Measurements

From the Raman spectroscopy tests, it can be concluded that a He-Cd laser of 325-nm wavelength (or shorter) as the excitation source is needed if residual stress in SiC structural layers is to be determined by this method. At that wavelength, the penetration depth of the 3C-SiC will only be 2.7 μm as compared to the much larger penetration depth for the 514.5-nm wavelength that was used here. This means that Raman backscattering will come from the first 1.35 μm of the surface being radiated. Any radiation penetrating further will be either absorbed or scattered. Since the thinnest layer, SiC-3, is only 1.5-μm thick, this should produce nice results. As explained in Section 3.1.3, the problem with fluorescence will still exist but, with better absorption, the Raman signal should overpower the electronic transitions.

Another recommendation for this test would be the use of a motorized microscope stage. With an automated stage, a beam on the chip can be scanned in steps of 1 μm. This is really essential to taking enough point scans to determine a good stress profile across the length of the beam, as it is impossible to have that kind of accuracy adjusting the stage by hand.

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If the opportunity arises, an item for future work would be to obtain a sample of bulk 3C-SiC for spectral characterization.

5.2 Release Process

Currently, FLX Micro, Inc. suggests using KOH as the etchant for the PolySi sacrificial layer. Since the chips used in this process had a several fabrication flaws and this being the first MUSiC^{SM} run, it is difficult to challenge such a suggestion with the results of this study. However, the one strong point of evidence to support such a change would be the reduced etch time with the $5(HNO_3):3(HF):3(CH_3COOH)$ acid dip.

This test provided the best opportunity for lessons learned. For example, the yield of viable MEMS device structures is increased dramatically when:

1) Agitation of partially released chips is avoided as much as possible with the use of chip holder or clamps
2) The use of the supercritical point CO_2 drying technique is used to eliminate surface tension forces on MEMS structures as the liquid CO_2 (which displaces the methanol) evaporates.

The release process also revealed a great deal about possible manufacturing flaws. The reddish-brown film seems to suggest either an incomplete CMP of the SiC-2 layer or incomplete cleaning after the CMP of SiC-2 layer. The inability to completely release the SiC-2 layer suggests that perhaps the SiC-1 layer was incompletely planarized. Variation in the color and texture of the SiC layers suggests poor process control, and variation in the deposition process will need to be controlled before the process is ready for market.

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Developing a precise and repeatable etch procedure for SiC MEMS would be a great area for future research.

5.3 Interferometry of Beam Arrays

The Zygo-interferometer test yielded some of the best results of this research. Had there been enough viable fixed-fixed beam arrays to work with, a better trend for the stress in at least the SiC3 layer could have been identified. Nevertheless, some useful information was extracted from the interferometer scans. In Figure 5.1, a comb drive in the SiC-3 layer is seen to be released and slightly bow up in the middle of the plate.

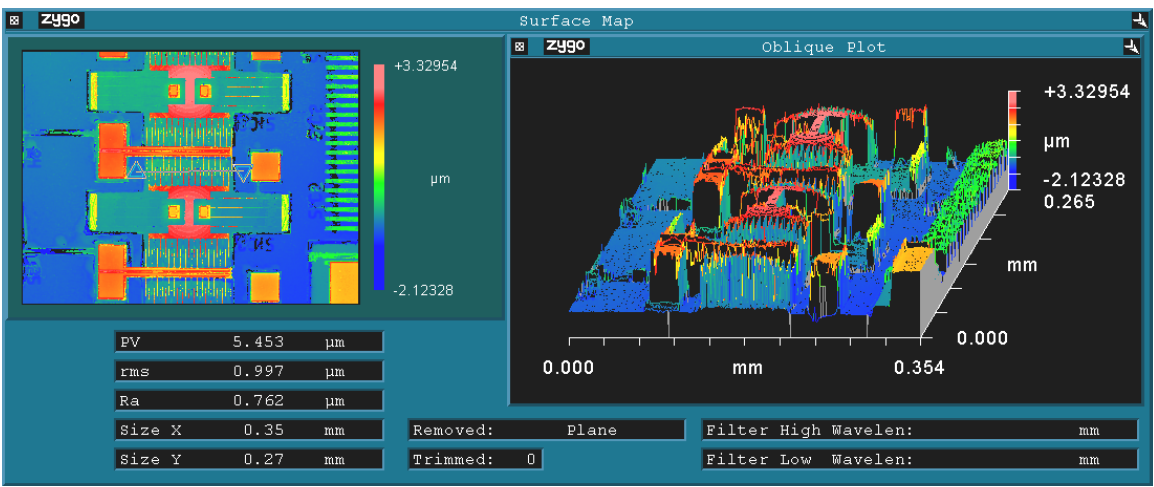

Figure 5.1: Zygo Interferometer profile of SiC-3

The surface plot in Figure 5.2 also shows how the teeth attached to the moving plate are bowed with the plate, while the stationary teeth are fairly level. It also demonstrates that the plate is not stuck down to the substrate, but is free to move. This

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profile could also aid in determining the amount of DC offset required to bring the teeth into alignment during a resonance test.

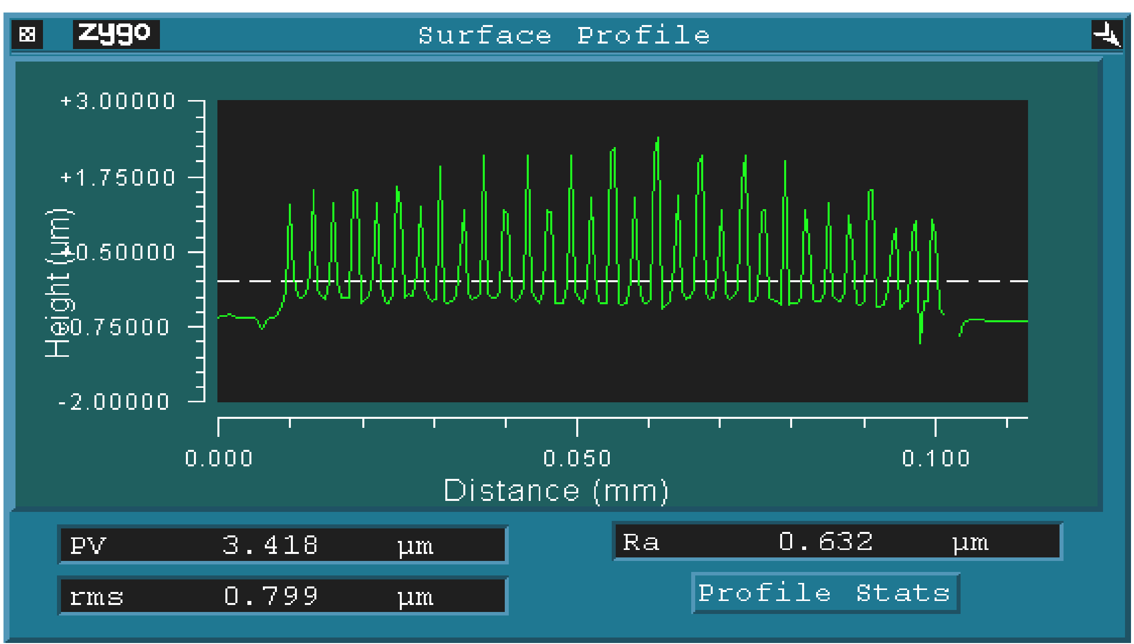

Figure 5.2: Surface profile across the teeth of a SiC3 comb drive

5.4 Comb-Drive Resonance Test

The resonance test failed to get the drive to move and, therefore, the comb-drive resonance test did not provide any useful data. Possible failure scenarios include: discontinuity between the nickel bond pads and the SiC structure; discontinuity between the different SiC layers; due to the stiffness of the material, 500V may not have been enough DC offset to move the drive. Before further tests are performed, electrical continuity between layers and bond pads should be tested. Furthermore, a value for the expected DC voltage offset should also be theoretically determined. With better test

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structures and further research, an AFIT student should pursue getting one of these comb drives to resonate.

5.5 Conclusion

Currently, the United States enjoys the benefits of having the strongest military not out of shear numbers of troops, but in the way it fights wars with advanced technology. High-temperature and extreme-environment semiconductors are essential to the continued enhancement of Department-of-Defense weapon and information systems, a core competency of U.S. military might. The work presented here is intended to further develop the budding technology of SiC MEMS devices manufactured with the MUSiC^{SM} process in support of Department-of-Defense weapon systems and industry. The success of this technology depends on accurate and nondestructive characterization methods of thin-film stress that causes device failure. To this end, the use of Raman spectroscopy as such a method was explored, and interferometry and comb-drive resonance tests were conducted to support any result found. Although the stress gradients were not detected due to lack of appropriate equipment, the research done here has laid the ground work for continued research in this area.

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Appendix A: Comb-Drive Test Setup

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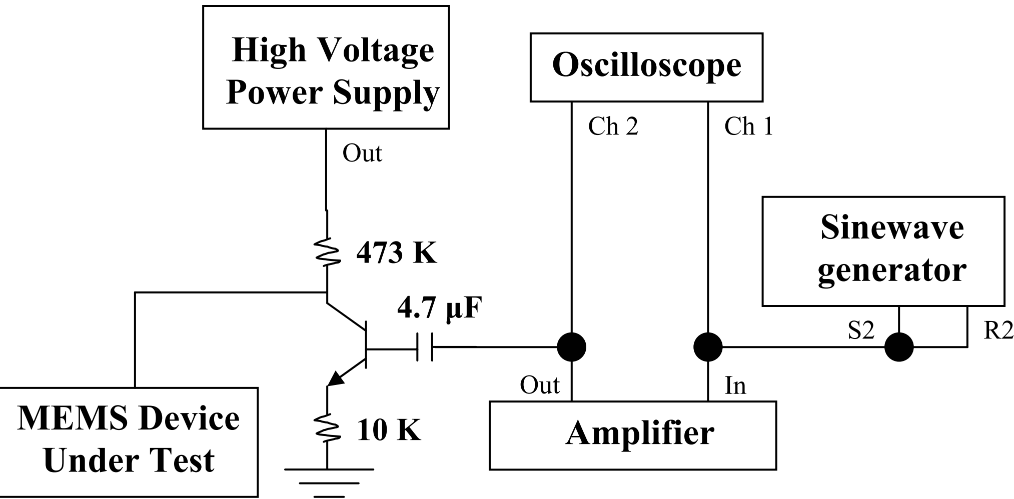
Appendix A: Comb Drive Resonant Test Setup



Note: the 4.7 µF capacitor needs to be an electrolytic capacitor to be able to handle at least 75 Volts.

Instrument settings:

Oscilloscope: channel 1 – 1 V/div, AC, Dual Mode, 20 msec Time/div (used to view generated sinewave from spectrum analyzer)
channel 2 – 5 V/div, AC (used to view output sinewave from amplifier should get ~30V p-p waveform)

Sinewave generator: Sinewave generator and resonance freq measurement
Port select T2/R2
Start Freq: 10 KHz, Resolution Bandwidth 300 Hz
Stop Freq; 30 KHz (The start/stop frequencies may have to be different as I'm not sure what your resonance should be.)
S2 = 15 dBm
R2 = 30 dBm
T2 = 20 dBm
Scale ref – Auto A and Auto B

High Voltage Power Supply:
V limit = 500 V,
Current limit = 5.25 mA
Set to adjust output Voltage
Set HV switch to on to get a voltage output. Leave off until ready to test and turn off as soon as test is completed. Be careful; there is a significant amount of Volts going through this circuit.

Amplifier:
Use channel 2 as channel 1 was inoperable. You need to get a maximum sinewave after the amp. This will be viewed on the channel 2 of the Oscilloscope.

Typical Voltages for the polysilicon resonators I tested were 30 V p-p sinewave at a 50-75 V DC level.

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Appendix B: Suggested Release Method from FLXMicro, Inc.

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MUSiC-1 Release Guidelines

November 22, 2002

Your MUSiC chips will require a combination release process since both polysilicon and silicon dioxide are used as sacrificial materials. While release times will vary from chip to chip based on specific design features (e.g. size and density of release holes, percent exposed area), the following guidelines should be helpful in identifying a process window for release. This information is based on trial releases performed earlier this week on other chips from the same run. Note that SiC is essentially impervious to the etchants used for release at these timescales, so is not likely to be damaged if it is necessary for you to exceed the recommended times.

Feel free to contact us with additional questions, problems, or concerns either by phone or e-mail to <melzak@fiberlead.com>.

1. Remove protective photoresist with acetone, Nano-strip, or other metal-safe resist stripper.

2. Perform first HF etch to remove oxide (thickness 0.75 to 1µm). Preferred etchant is undiluted 49% HF.

3. Perform KOH etch to remove polysilicon (thickness ~2µm). TMAH or XeF_2 may be used as alternative silicon etch chemicals. The etch is observed to be complete when:
    a. Underlying green oxide is visible,
    b. Few, if any, bubbles are seen, and
    c. Any residual SiC-3 in the field region that was not removed during RIE etching lifts off (for most chips this will not be an issue).

    For 20% (w/w) KOH at 65°C polysilicon removal took between 10 and 40 minutes. Note that the silicon substrate will be etched at the chip edges, which become exposed during wafer dicing.

4. Perform final HF etch to remove oxide (thickness ~2µm). Upon release completion, the underlying purple nitride layer should be visible. With 49% HF, this step required at least 8 minutes to complete.

5. Supercritical CO_2 drying may be helpful as a final step, although we have released devices successfully without requiring this.

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Appendix C: MathCAD Calculations

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Appendix C: Calculations for Comb Drive Frequency Test
SiC-2 Layer Comb Drives

Definitions and Parameters: $\mu m := 10^{-6} \cdot m$ $\quad GPa := 10^{9} \cdot Pa$

Density of SiC: $\rho := 3.17 \cdot \frac{gm}{cm^3}$

Thickness: $d_{SiC2} := 2.0 \cdot \mu m$

Mass of Truss: 2 Trusses

$H_T := 15 \cdot \mu m$ $\quad W_T := (16 + 16 + 34) \cdot \mu m$

$V_{Trusses} := 2 \cdot H_T \cdot W_T \cdot d_{SiC2}$ $\quad V_{Trusses} = 3.96 \times 10^{-15}\,\mathrm{m}^3$

$M_t := V_{Trusses} \cdot \rho$ $\quad M_t = 1.2553 \times 10^{-11}\,\mathrm{kg}$

Mass of Beams: 12 beams

$H_B := 100 \cdot \mu m$ $\quad W_B := 2.0 \cdot \mu m$

$V_{beams} := 12 \cdot H_B \cdot W_B \cdot d_{SiC2}$ $\quad V_{beams} = 4.8 \times 10^{-15}\,\mathrm{m}^3$

$M_b := V_{beams} \cdot \rho$ $\quad M_b = 1.5216 \times 10^{-11}\,\mathrm{kg}$

Mass of Plate:

interior teeth: (13 on each side)

$H_{inTeeth} := 3.0 \cdot \mu m$ $\quad W_{inTeeth} := 40 \cdot \mu m$

$V_{inTeeth} := \left(d_{SiC2} \cdot H_{inTeeth} \cdot W_{inTeeth}\right) \cdot 2 \cdot 13$ $\quad V_{inTeeth} = 6.24 \times 10^{-15}\,\mathrm{m}^3$

outside teeth: (2 on each side)

$H_{outTeeth} := 3.0 \cdot \mu m$ $\quad W_{outTeeth} := 52 \cdot \mu m$

$V_{outTeeth} := \left(d_{SiC2} \cdot H_{outTeeth} \cdot W_{outTeeth}\right) \cdot 2 \cdot 2$ $\quad V_{outTeeth} = 1.248 \times 10^{-15}\,\mathrm{m}^3$

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plate hub:

$H_{hub} := 20 \cdot \mu m$ $\quad W_{hub} := 54 \cdot \mu m$

$V_{hub} := (d_{SiC2} \cdot H_{hub} \cdot W_{hub})$ $\quad V_{hub} = 2.16 \times 10^{-15}\ m^3$

inside arm: (1 on each side)

$H_{inArm} := 90 \cdot \mu m$ $\quad W_{inArm} := 17 \cdot \mu m$

$V_{inArm} := (d_{SiC2} \cdot H_{inArm} \cdot W_{inArm}) \cdot 2$ $\quad V_{inArm} = 6.12 \times 10^{-15}\ m^3$

outside arm: (1 on each side)

$H_{outArm} := 165 \cdot \mu m$ $\quad W_{outArm} := 12 \cdot \mu m$

$V_{outArm} := (d_{SiC2} \cdot H_{inArm} \cdot W_{inArm}) \cdot 2$ $\quad V_{outArm} = 6.12 \times 10^{-15}\ m^3$

$V_{plate} := V_{inTeeth} + V_{outTeeth} + V_{hub} + V_{inArm} + V_{outArm}$ $\quad V_{plate} = 2.1888 \times 10^{-14}\ m^3$

$M_p := V_{plate} \cdot \rho$ $\quad M_p = 6.9385 \times 10^{-11}\ kg$

Cross sectional moment of inertia, I_z :

$b := d_{SiC2}$ $\quad h := W_B$ $\quad I_z := \frac{b \cdot h^3}{12}$ $\quad I_z = 1.3333 \times 10^{-24}\ m^4$

Governing Equation:

$$f = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{k_x}{M}} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{24 \cdot E \cdot I_z}{\left(M_p + \frac{1}{4} \cdot M_t + \frac{12}{35} \cdot M_b\right) \cdot L^3}}$$

Length of Beams: $\quad L := H_B$

$f :=$ ▮

Solve for E:

$$E := \frac{1}{840} \cdot (140 \cdot M_p + 35 \cdot M_t + 48 \cdot M_b) \cdot L^3 \cdot f^2 \cdot \frac{\pi^2}{I_z}$$

$E :=$ ▮

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Estimate from other source:

Given a modulus of $E = 329 \cdot GPa$ for polycrystalline SiC

modulus source: http://www-mat.ee.tu-berlin.de/research/sic_elast/sic_elas.htm

$$f(E) := \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{24 \cdot E \cdot I_z}{\left(M_p + \frac{1}{4} \cdot M_t + \frac{12}{35} \cdot M_b\right) \cdot L^3}}$$

$$f(329 \cdot GPa) = 58.5693\,kHz$$

$$f(307 \cdot GPa) = 56.5772\,kHz \qquad f(448 \cdot GPa) = 68.3457\,kHz$$

$$\frac{V_{plate} + V_{beams} + V_{Trusses}}{d_{SiC2}} = 15324\,\mu m^2$$

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Appendix C: Calculations for Comb Drive Frequency Test
SiC-3 Layer Comb Drives

Definitions and Parameters: $\mu m := 10^{-6} \cdot m$ $\quad GPa := 10^{9} \cdot Pa$

Density of SiC: $\rho := 3.17 \cdot \frac{gm}{cm^3}$

Thickness: $d_{SiC3} := 1.5 \cdot \mu m$

Mass of Truss: 2 Trusses

$H_T := 15 \cdot \mu m$ $\quad W_T := 78 \cdot \mu m$

$V_{Trusses} := 2 \cdot H_T \cdot W_T \cdot d_{SiC3}$ $\quad V_{Trusses} = 3.51 \times 10^{-15} m^3$

$M_t := V_{Trusses} \cdot \rho$ $\quad M_t = 1.11267 \times 10^{-11} kg$

Mass of Beams: 12 beams

$H_B := 150 \cdot \mu m$ $\quad W_B := 2.0 \cdot \mu m$

$V_{beams} := 12 \cdot H_B \cdot W_B \cdot d_{SiC3}$ $\quad V_{beams} = 5.4 \times 10^{-15} m^3$

$M_b := V_{beams} \cdot \rho$ $\quad M_b = 1.7118 \times 10^{-11} kg$

Mass of Plate:

teeth: (15 on each side)

$H_{inTeeth} := 3.0 \cdot \mu m$ $\quad W_{inTeeth} := 40 \cdot \mu m$

$V_{inTeeth} := (d_{SiC3} \cdot H_{inTeeth} \cdot W_{inTeeth}) \cdot 2 \cdot 15$ $\quad V_{inTeeth} = 5.4 \times 10^{-15} m^3$

plate hub:

$H_{hub} := 20 \cdot \mu m$ $\quad W_{hub} := 54 \cdot \mu m$

$V_{hub} := (d_{SiC3} \cdot H_{hub} \cdot W_{hub})$ $\quad V_{hub} = 1.62 \times 10^{-15} m^3$

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inside arm: (1 on each side)

$H_{inArm} := 90 \cdot \mu m$ $\quad$ $W_{inArm} := 17 \cdot \mu m$

$V_{inArm} := \left(d_{SiC3} \cdot H_{inArm} \cdot W_{inArm}\right) \cdot 2$ $\quad$ $V_{inArm} = 4.59 \times 10^{-15} m^3$

outside arm: (1 on each side)

$H_{outArm} := 171 \cdot \mu m$ $\quad$ $W_{outArm} := 12 \cdot \mu m$

$V_{outArm} := \left(d_{SiC3} \cdot H_{inArm} \cdot W_{inArm}\right) \cdot 2$ $\quad$ $V_{outArm} = 4.59 \times 10^{-15} m^3$

$V_{plate} := V_{inTeeth} + V_{hub} + V_{inArm} + V_{outArm}$ $\quad$ $V_{plate} = 1.62 \times 10^{-14} m^3$

$M_p := V_{plate} \cdot \rho$ $\quad$ $M_p = 5.1354 \times 10^{-11} kg$

Cross sectional moment of inertia, I_z :

$b := d_{SiC3}$ $\quad$ $h := W_B$ $\quad$ $I_z := \frac{b \cdot h^3}{12}$ $\quad$ $I_z = 1 \times 10^{-24} m^4$

Governing Equation:

$$f = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{k_x}{M}} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{24 \cdot E \cdot I_z}{\left(M_p + \frac{1}{4} \cdot M_t + \frac{12}{35} \cdot M_b\right) \cdot L^3}}$$

Length of Beams:

$L := H_B$ $\quad$ $f :=$ ▮

Solve for E:

$$E := \frac{1}{840} \cdot \left(140 \cdot M_p + 35 \cdot M_t + 48 \cdot M_b\right) \cdot L^3 \cdot f^2 \cdot \frac{\pi^2}{I_z}$$

$E :=$ ▮

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Estimate from other source:

Given a modulus of $E = 329 \cdot GPa$ for polycrystalline SiC

modulus source: http://www-mat.ee.tu-berlin.de/research/sic_elast/sic_elas.htm

$$f(E) := \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{24 \cdot E \cdot I_z}{\left(M_p + \frac{1}{4} \cdot M_t + \frac{12}{35} \cdot M_b\right) \cdot L^3}}$$

$$f(329 \cdot GPa) = 31.42637\,kHz$$

$$f(307 \cdot GPa) = 30.35746\,kHz \qquad f(448 \cdot GPa) = 36.67205\,kHz$$

$$\frac{V_{plate} + V_{beams} + V_{Trusses}}{d_{SiC3}} = 16740\,\mu m^2$$

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Appendix C: Calculations for Fixed-Fixed Beam Arrays in the SiC-3 Layer

Equation 2: $L = \sqrt{\dfrac{\pi^2 t^2 E}{3\sigma}} \quad (\mu m)$

$\mu m := 10^{-6} \cdot m$

$GPa := 10^{9} \cdot Pa$

$MPa := 10^{6} \cdot Pa$

$E := 329 \cdot GPa$

$t := 1.5 \cdot \mu m$

$$\sigma(L) := \frac{\pi^2 \cdot t^2 \cdot E}{3 \cdot L^2}$$

$\sigma(170 \cdot \mu m) = 84.267\, MPa$

$\sigma(110 \cdot \mu m) = 201.267\, MPa$

$\sigma(180 \cdot \mu m) = 75.164\, MPa$

$\sigma(190 \cdot \mu m) = 67.461\, MPa$

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14. ABSTRACT

During the fabrication of Micro-Electro-Mechanical Systems (MEMS), residual stress is often induced in the thin films that are deposited to create these systems. These stresses can cause the device to fail due to buckling, curling, or fracture. Government and industry are looking for ways to characterize the stress during the deposition of thin films in order to reduce or eliminate device failure. Micro-Raman spectroscopy has been successfully used to analyze poly-silicon MEMS devices made with the Multi-User MEMS Process (MUMPS®). Micro-Raman spectroscopy was selected because it is nondestructive, fast and has the potential for *in situ* stress monitoring. This research attempts to validate the use of Raman spectroscopy to analyze the stress in MEMS made of silicon carbide (SiC) using the Multi-User Silicon Carbide surface micromachining (MUSiC^{SM}) process. Surface interferometry of fixed-fixed beam arrays and comb drive resonance test are employed to determine stress and compare it to the Raman values. Research also includes baseline spectra of 6H, 4H, and 15R poly-types of bulk SiC. Raman spectra of 1- to 2-μm thick 3C-SiC thin films deposited on silicon, silicon nitride, and silicon oxide substrates are presented as an attempt to establish a baseline spectra for 3C-SiC, the poly-type of SiC found in MEMS made with the MUSiC^{SM} process.

15. SUBJECT TERMS

Microelectromechanical Systems, MEMS, Raman Spectroscopy, MUSiC, MUSiC^{SM}, Silicon Carbide, SiC, Surface Micromachining, Comb-drive resonance, Zygo Interferometry, Thin-film stress, Bulk SiC Raman Spectra, APCVD, Wet etching, MEMS release.

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